

Compal Confidential

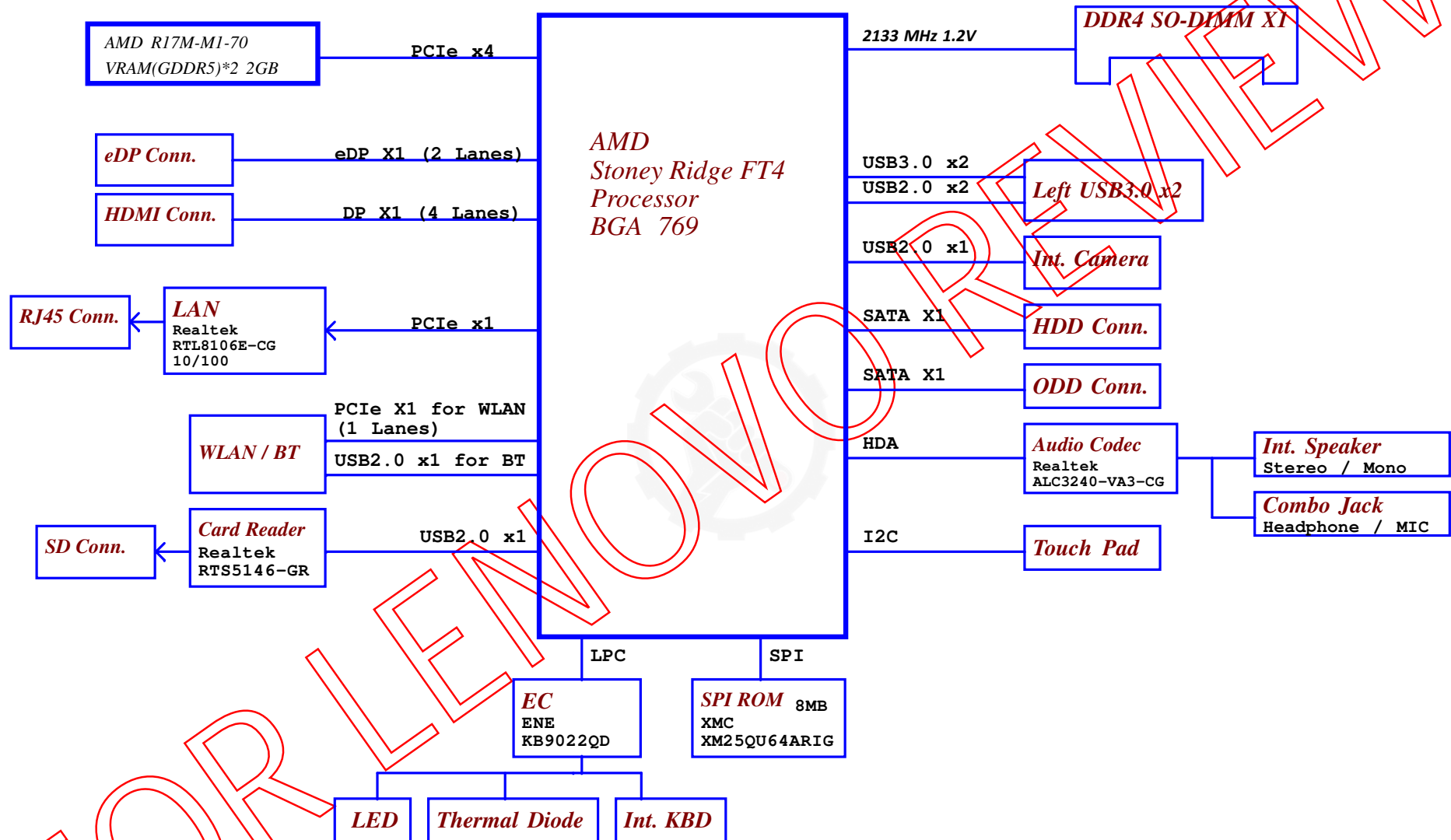
DIS M/B Schematics Document

AMD Stoney Ridge FT4

LA-G241P
2018-03-12
REV : 1 . 0

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Issued Date	2018/03/12	Deciphered Date	2019/03/12	Title	
				Cover Page	
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AMD Stoney Ridge FT4



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APU PCIE PORT LIST

Port	Device
0	LAN
1	
2	WLAN
3	

BOM Structure Table

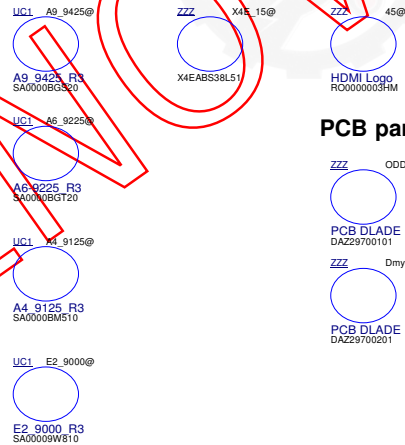
[illegible]

USB 3.0	USB 2.0	3 External USB Port
	0	
	1	WLAN/BT Combo
	2	Camera
	3	Card Reader
	4	
1	5	Left USB3.0 port 1
2	6	Left USB3.0 port 2
	7	

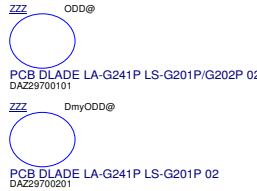
OC#	USB Port	
0		
1	USB2 port5	USB3 port1
2		
3		

APU part ~~X4E level BOM~~ HDMI logo

APU part ~~**X4E level BOM**~~ **HDMI logo**



PCB part



Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+0.95VALW	0.95V always on power rail	ON	ON	ON
+0.95VS	0.95V switched power rail	ON	OFF	OFF
+1.2V	1.2V power rail for APU and DDR	ON	ON	OFF
+2.5V	2.5V switched power rail for DDR	ON	ON	OFF
+0.6V	0.6V switched power rail for DDR terminator	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVBATT	RTC power	ON	ON	ON
+0.775VALW	0.775V always on power rail	ON	ON	ON

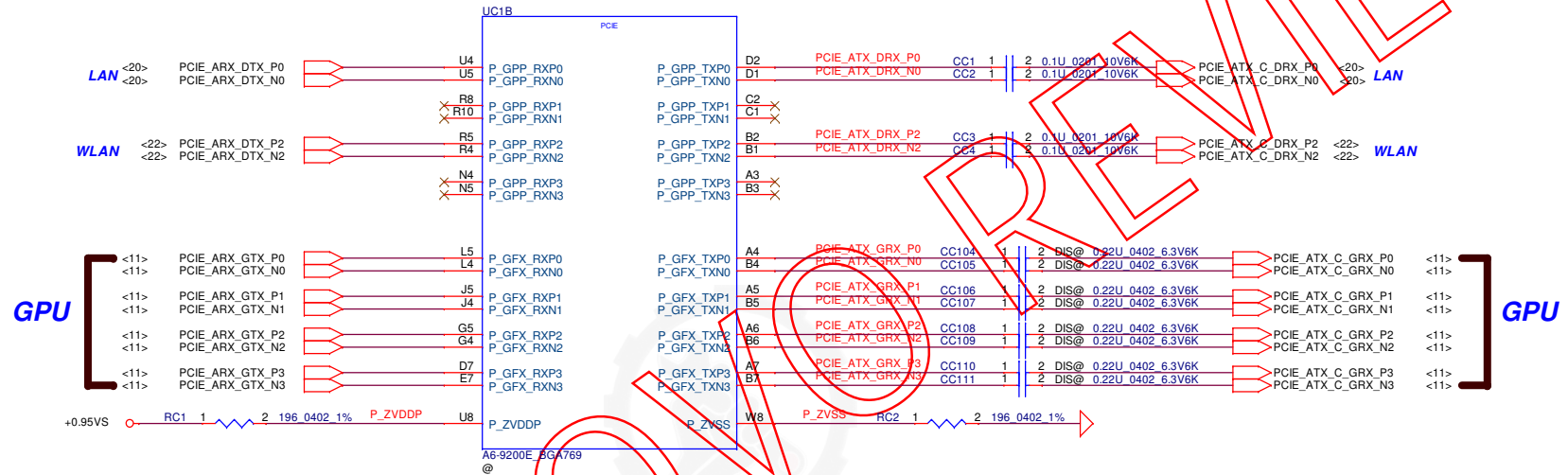
	SOURCE	APU	BATT	NPCE388N	SO-DIMM	WLAN	Thermal Sensor
EC_SMB_CK1 EC_SMB_DA1	ENE9022 +3VL	X	V +3VALW	X	X	X	X
APU_SCLK0 APU_SDATA0	APU +3VS	X	X	X	V +3VS	X	X
EC_SMB_CK2 EC_SMB_DA2	ENE9022 +3VS	V +1.8VS	X	X	X	X	V +3VS

EC SM Bus2 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011x b	16H	APU	1001 100X b	98H
Charger	0001 0010 b	12H			

GPU SM Bus address

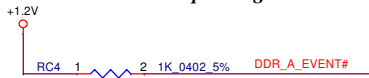
Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1010 000X b	A0H	GPU	0100 0001 b	0X41H



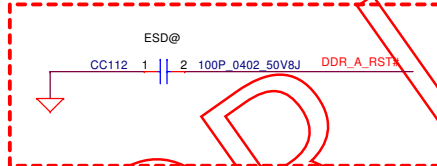
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EVENT# pull high



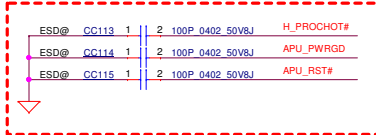
ESD



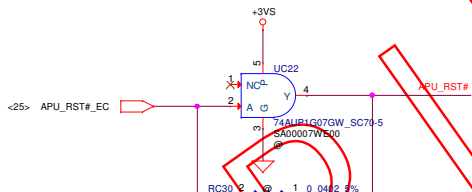
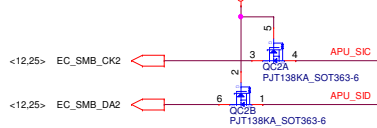
Place them close to APU within 1"

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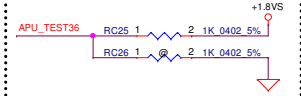
ESD



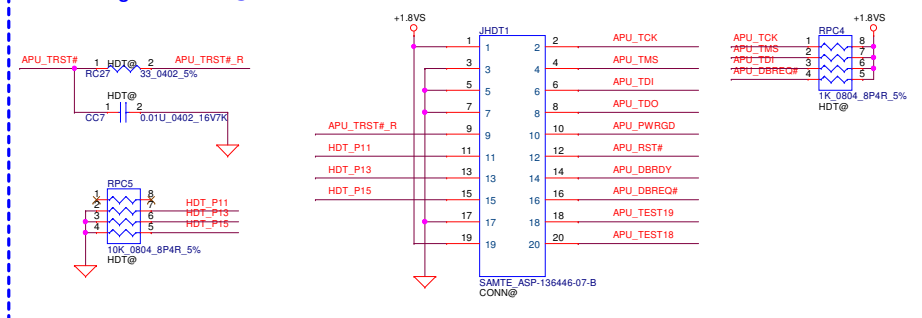
PU on EC side



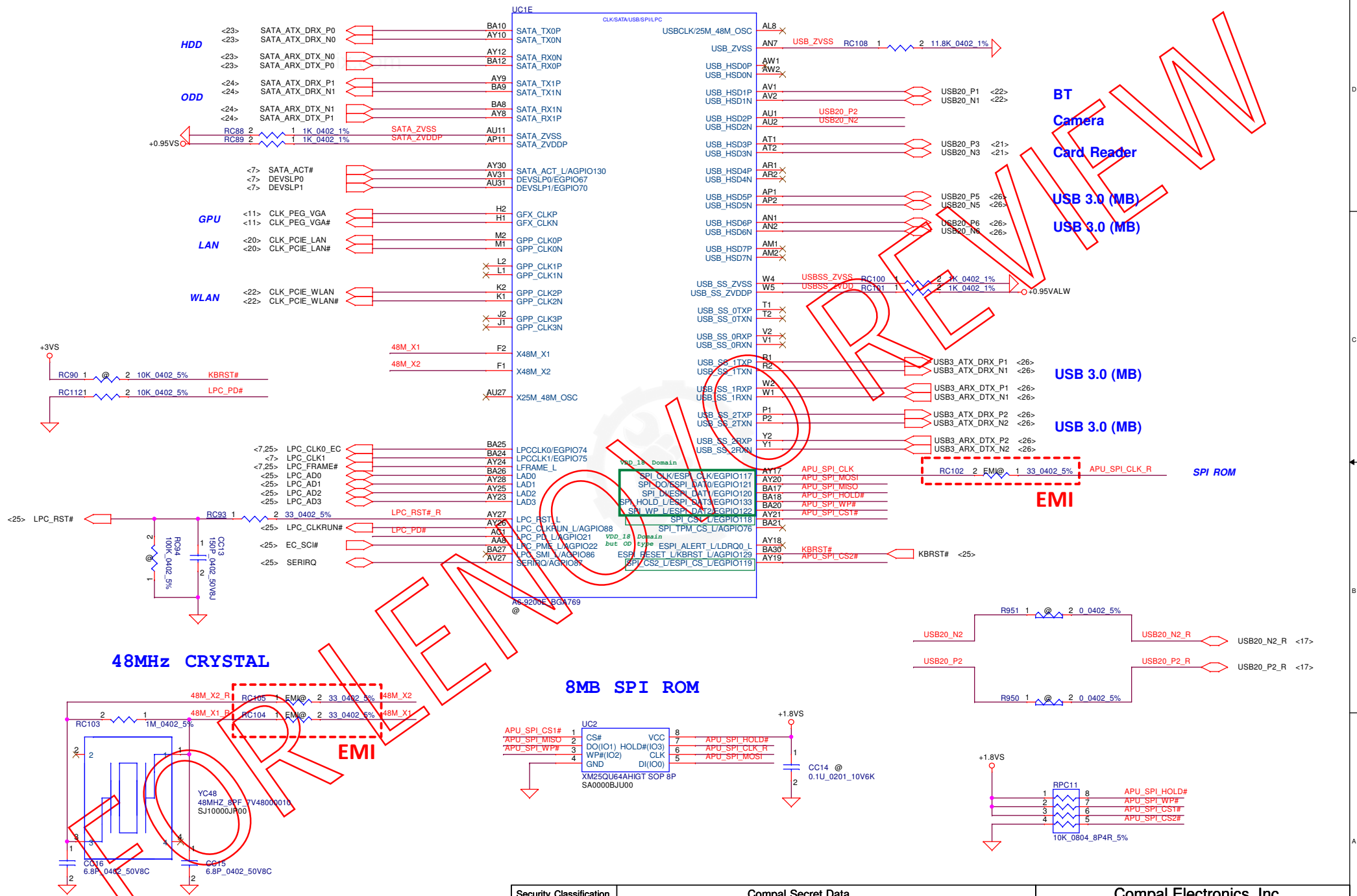
Stoney Ridge FP4_FT4 Interlock July_2017 ver 2.1:
To enable HDMI, it must be pulled up to 1.8V_50 rail
by 1K ohm resistor



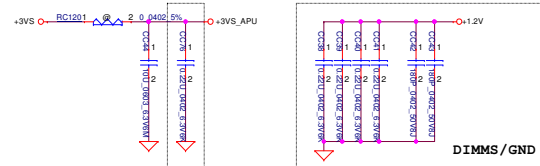
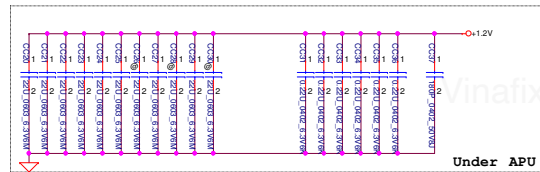
HDT+ Debug conn - HDT@



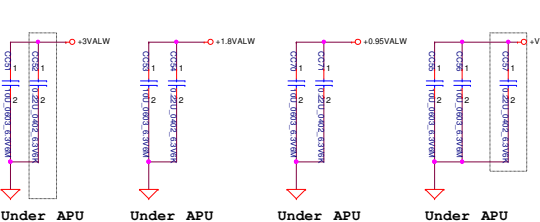
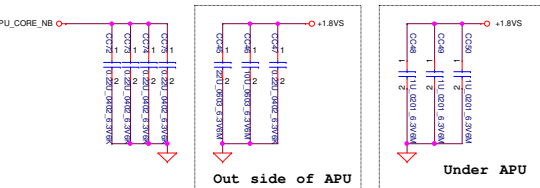
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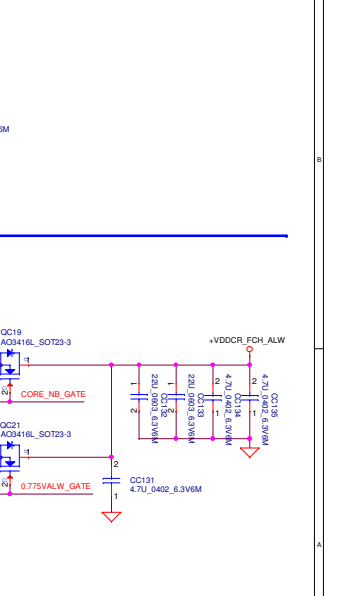
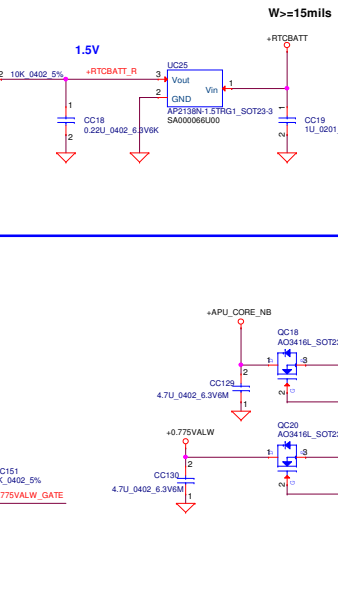
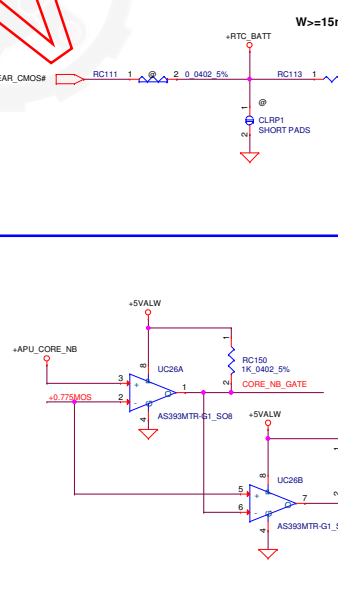
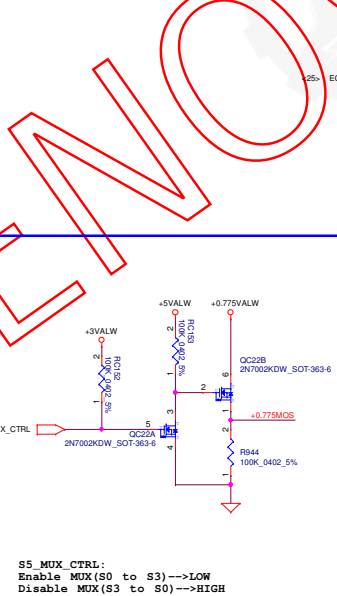
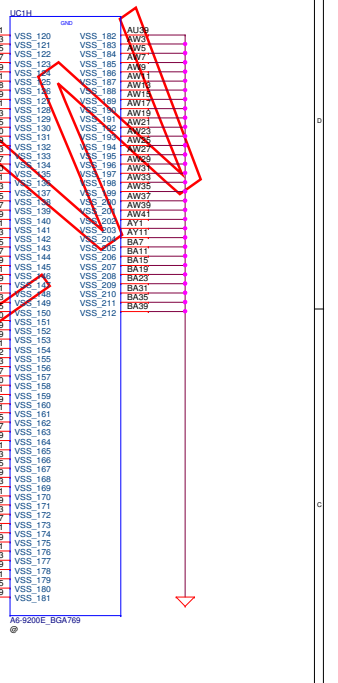
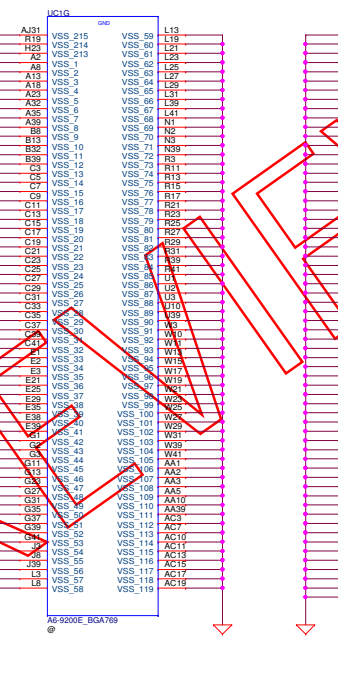
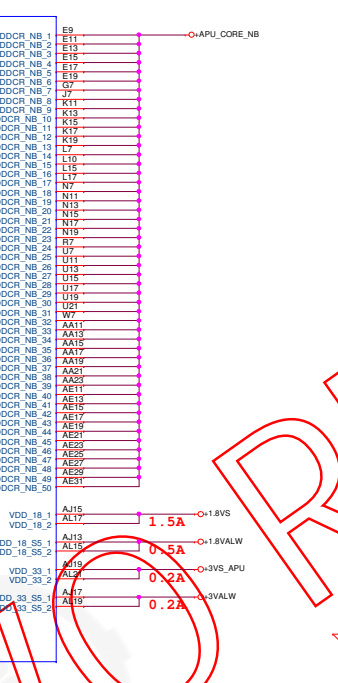
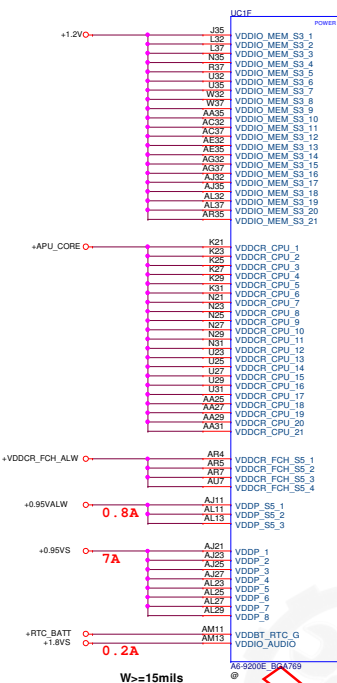
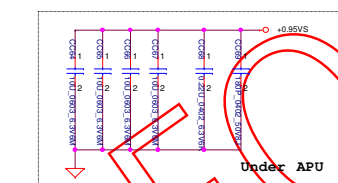
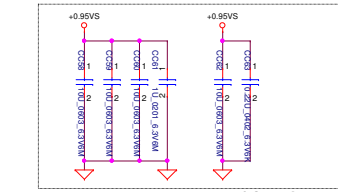
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Under APU ACROSS +1.2V_VDDQ AND VSS SPLIT



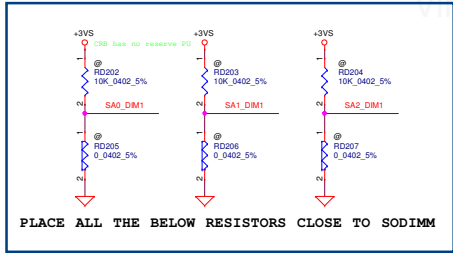
+0.95VS OF APU



S5_MUX_CTRL:
Enable MUX (S0 to S3)--->LOW
Disable MUX (S3 to S0)--->HIGH

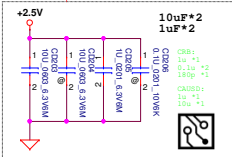
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Stoney So-DIMM1

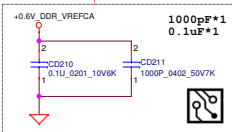


SPD ADDRESS FOR CHANNEL A :
SA0 = 0; SA1 = 0; SA2 = 0.

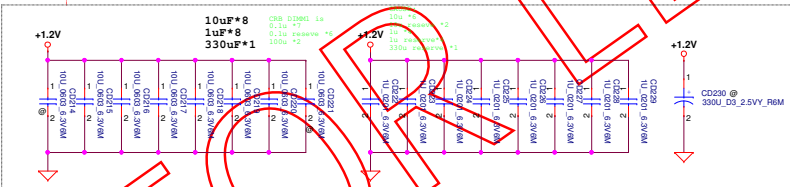
Layout Note:
Place near JDIMM1.257,259



Layout Note:
PLACE THE CAP near JDIMM1. 164

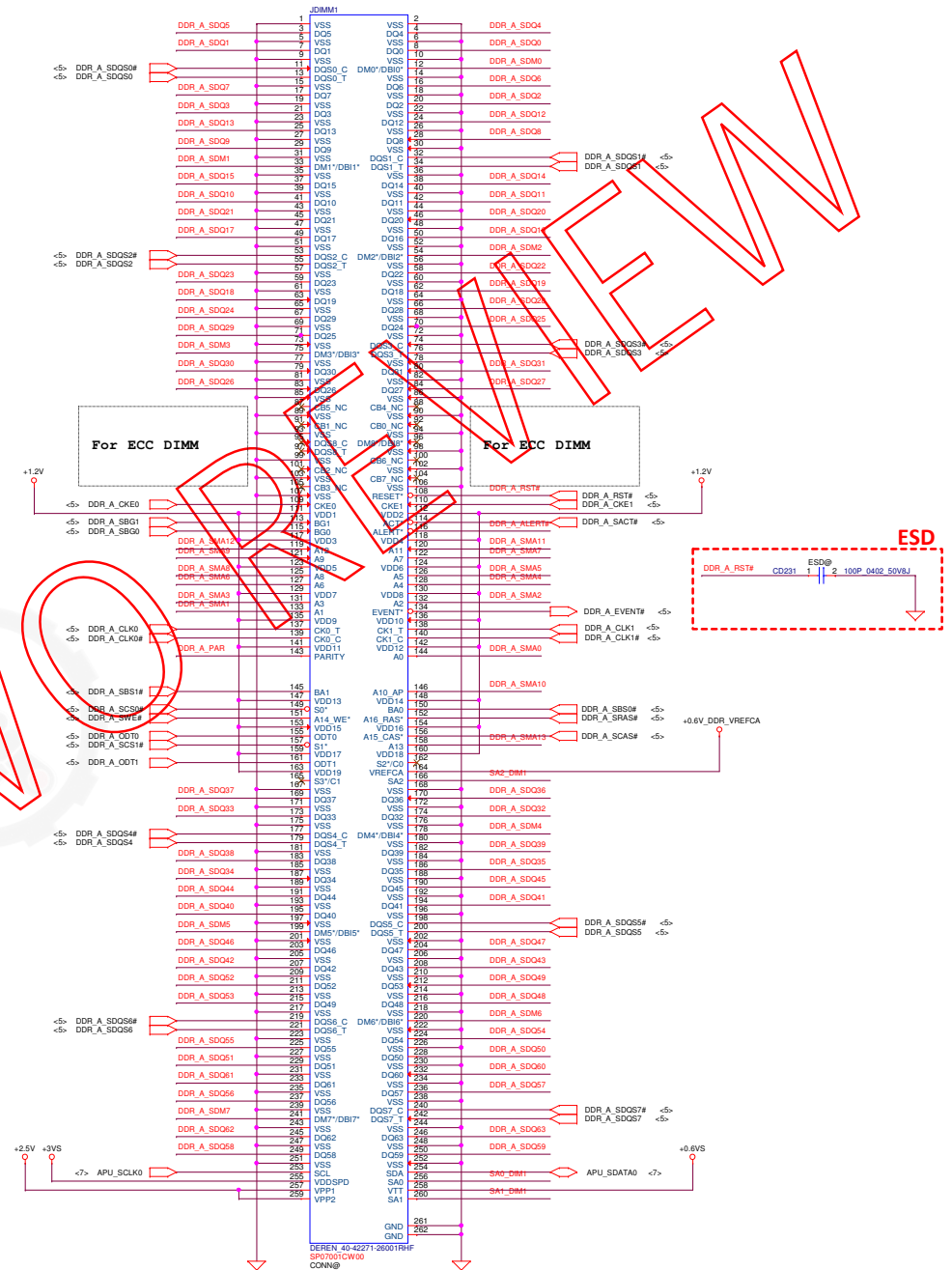
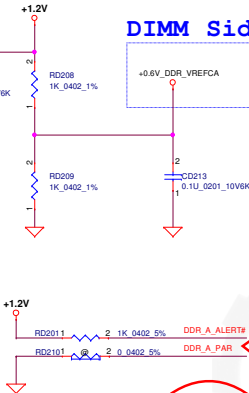


Layout Note:
Place near JDIMM1

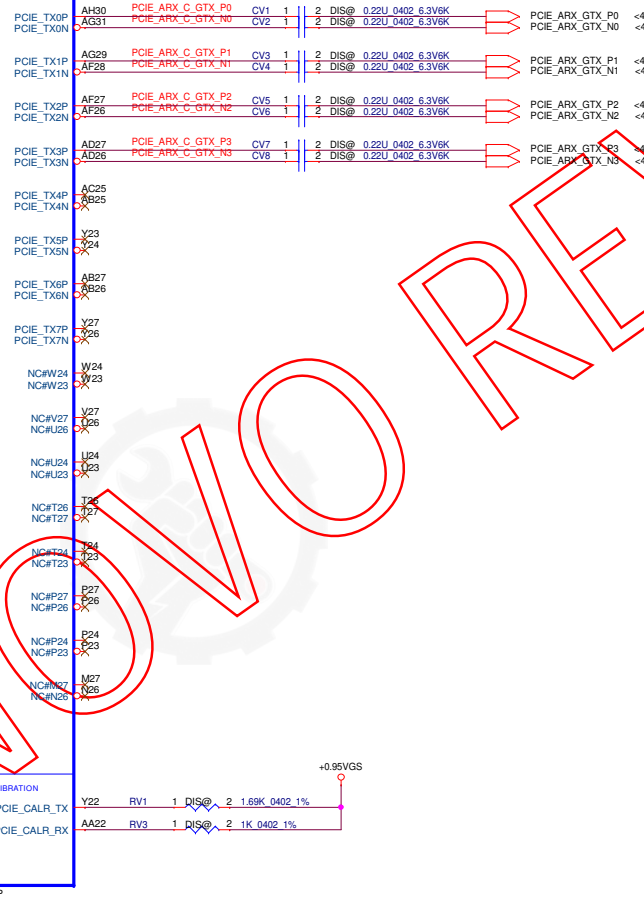
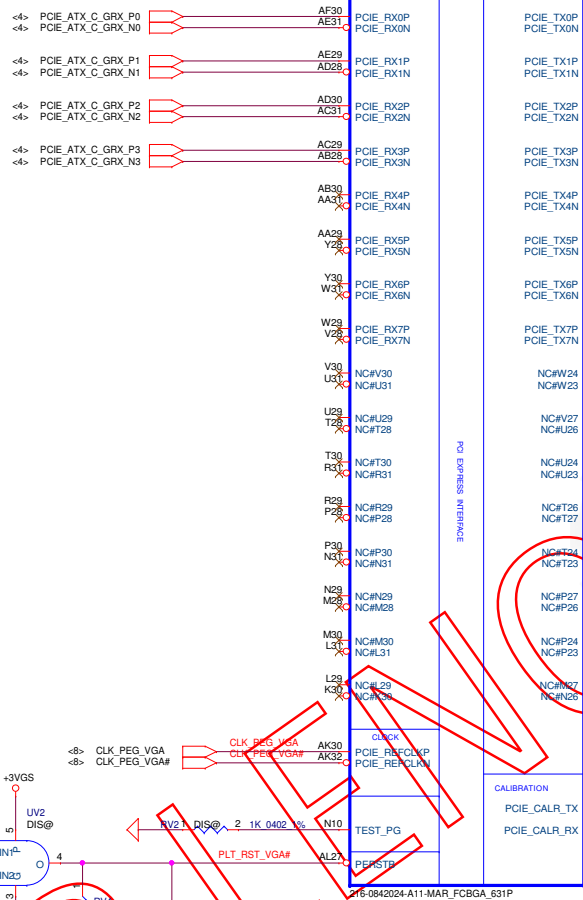


<5> DDR_A_SQ0[63..0]
<5> DDR_A_SDM[7..0]
<5> DDR_A_SMA[13..0]

DIMM Side

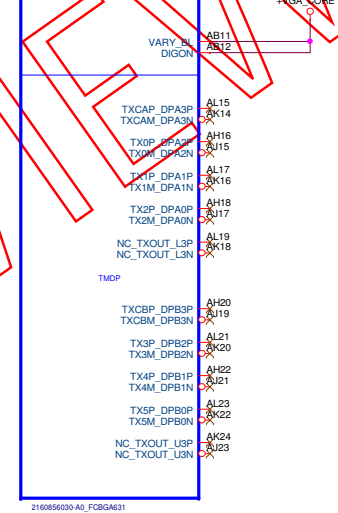


UV1A DIS@



No Use GPU Display Port output

UV1F DIS@



RV3153 2 @DIS@ 1 100K 0402 5% PXS_RST#

PXS_RST#

APU_PCIE_RST#

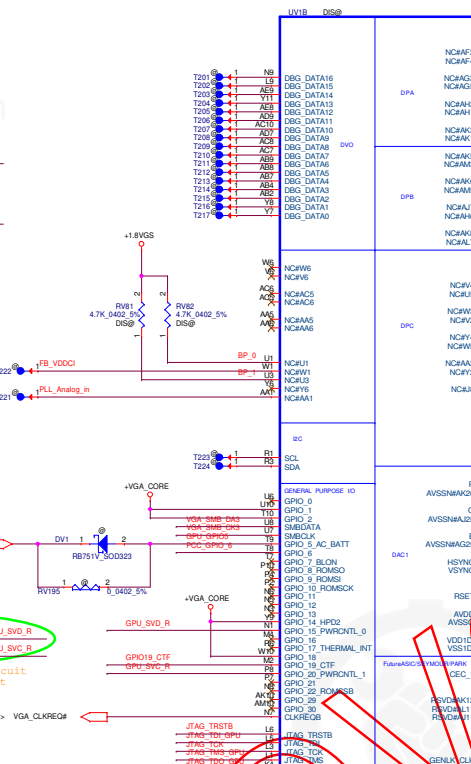
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MC74VHC1G08DFT2G_SC70-5

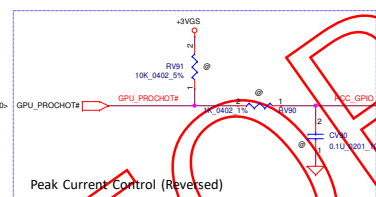
RV4 100K 0402 5% DIS@

PLT_RST_VGA#

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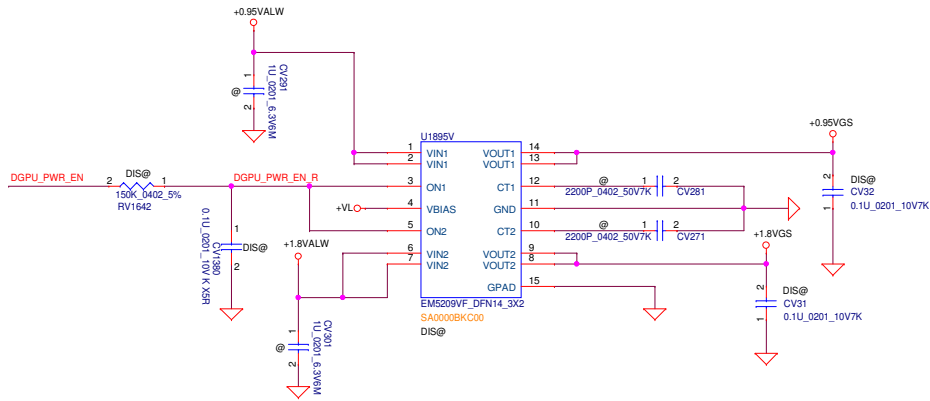
Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11



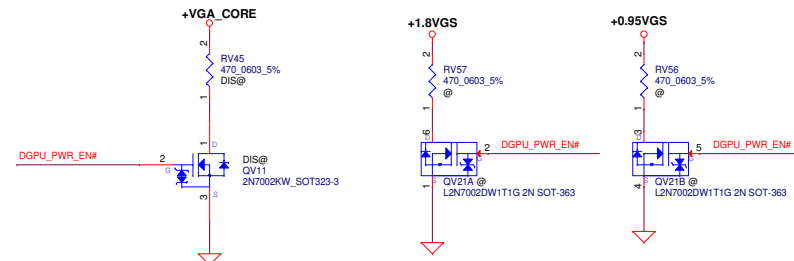
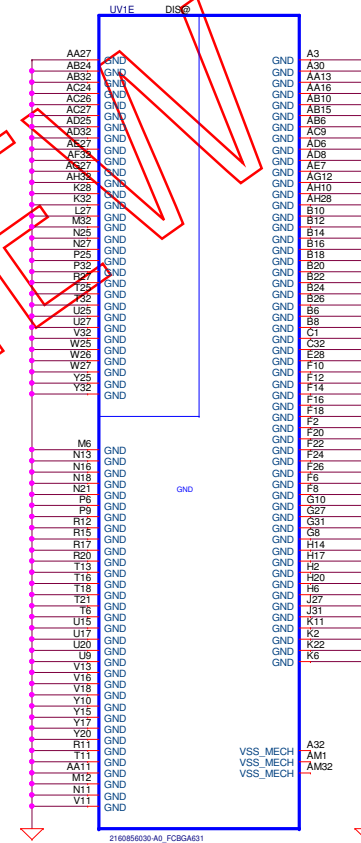
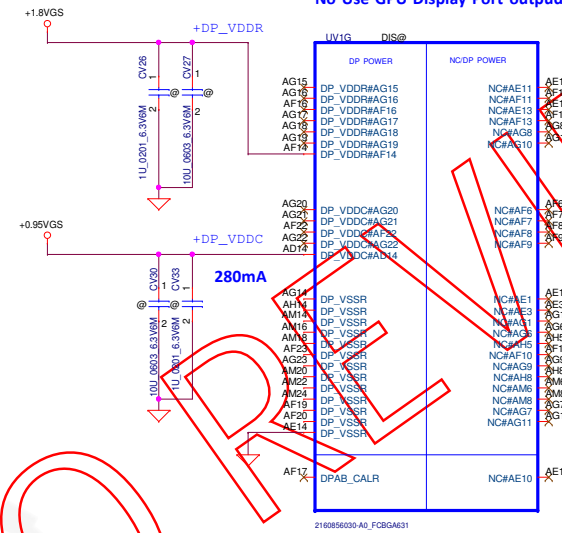
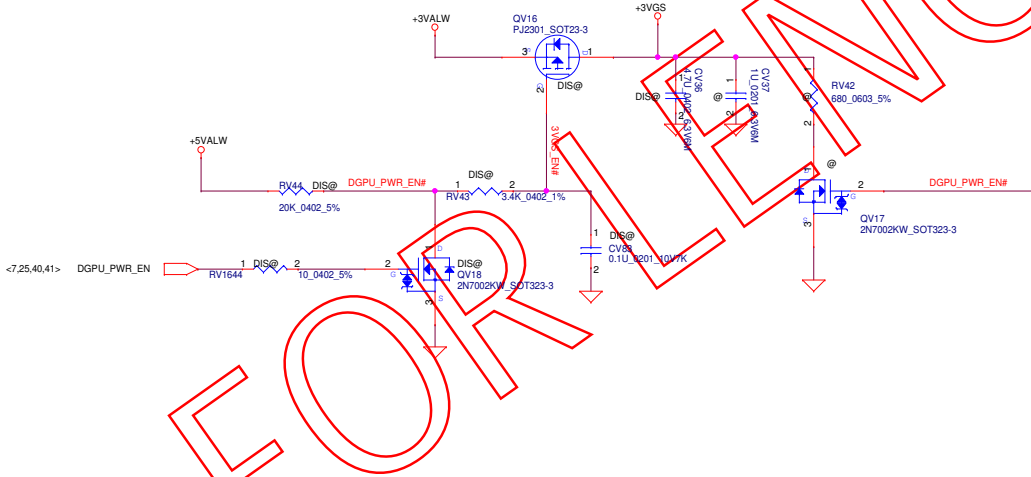
SVC	SVD	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

+1.8VALW TO +1.8VGS
+0.95VALW TO +0.95VGS
Load switch

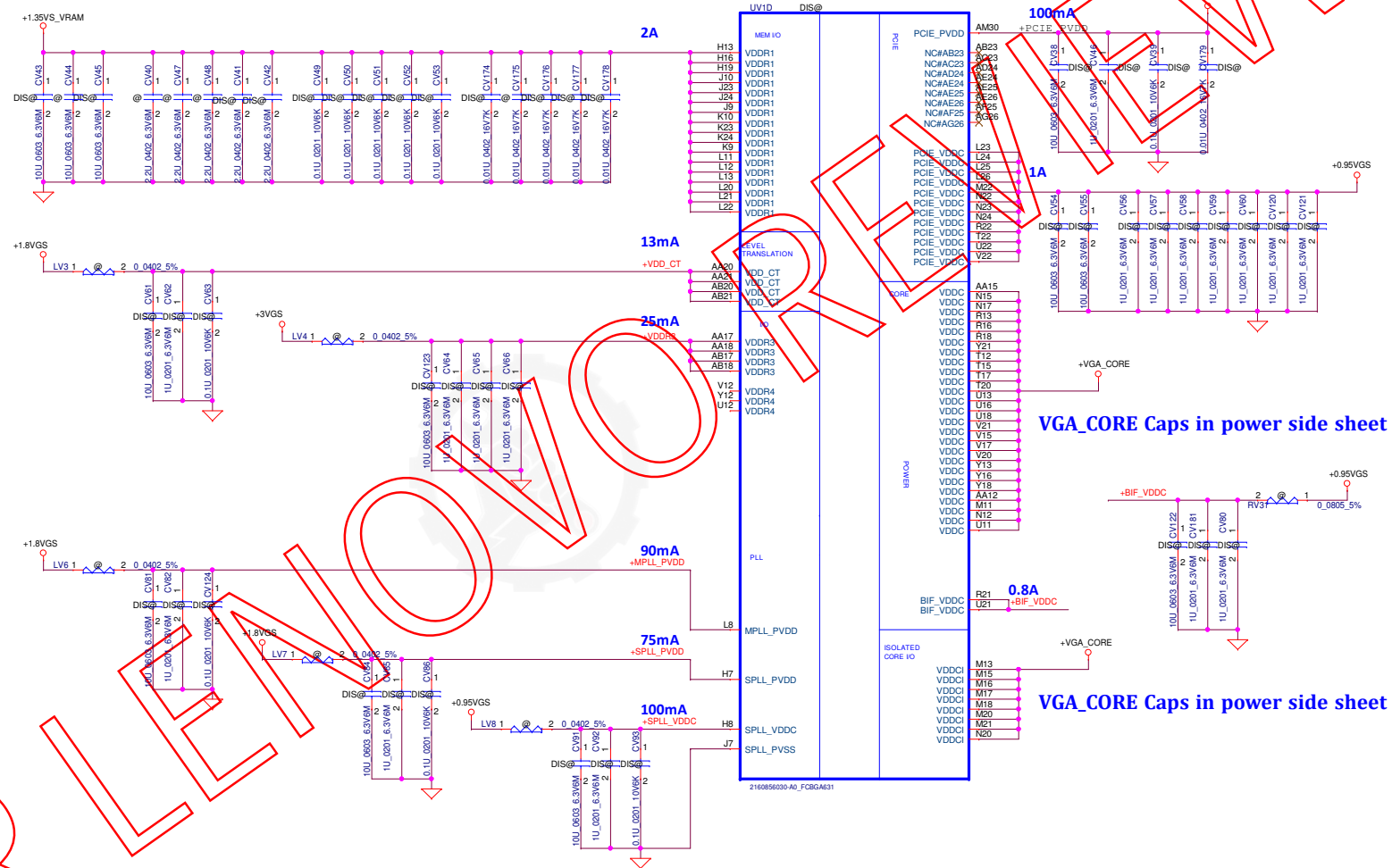
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+3VALW to +3VGS



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VGA_CORE Caps in power side sheet

VGA_CORE Caps in power side sheet

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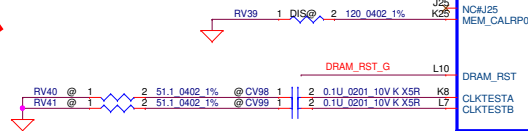


Diagram illustrating the interconnectivity of various components, primarily focusing on the **DDR5** memory interface and associated control logic.

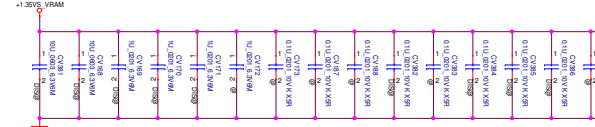
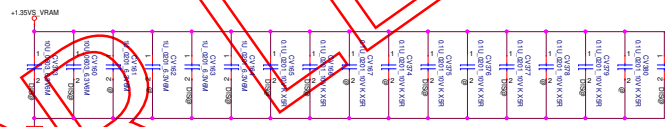
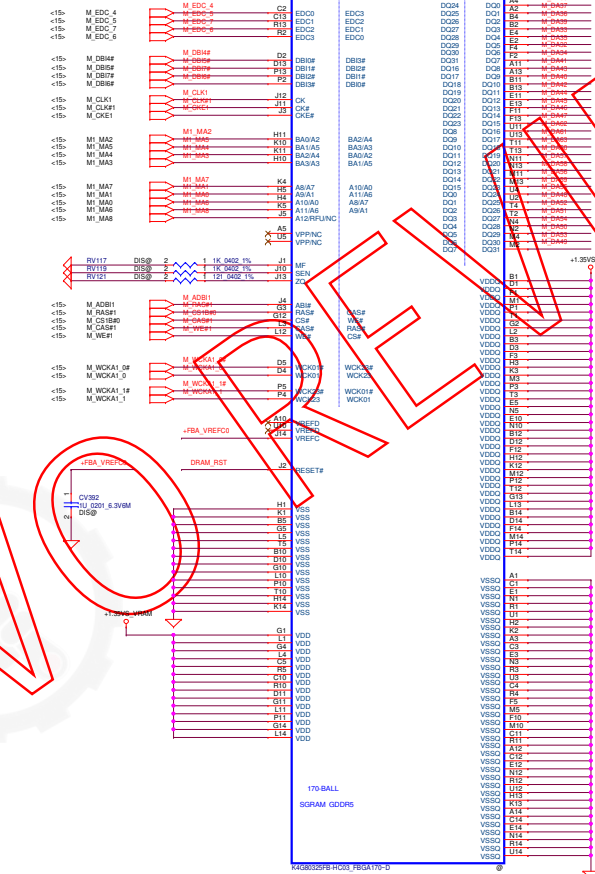
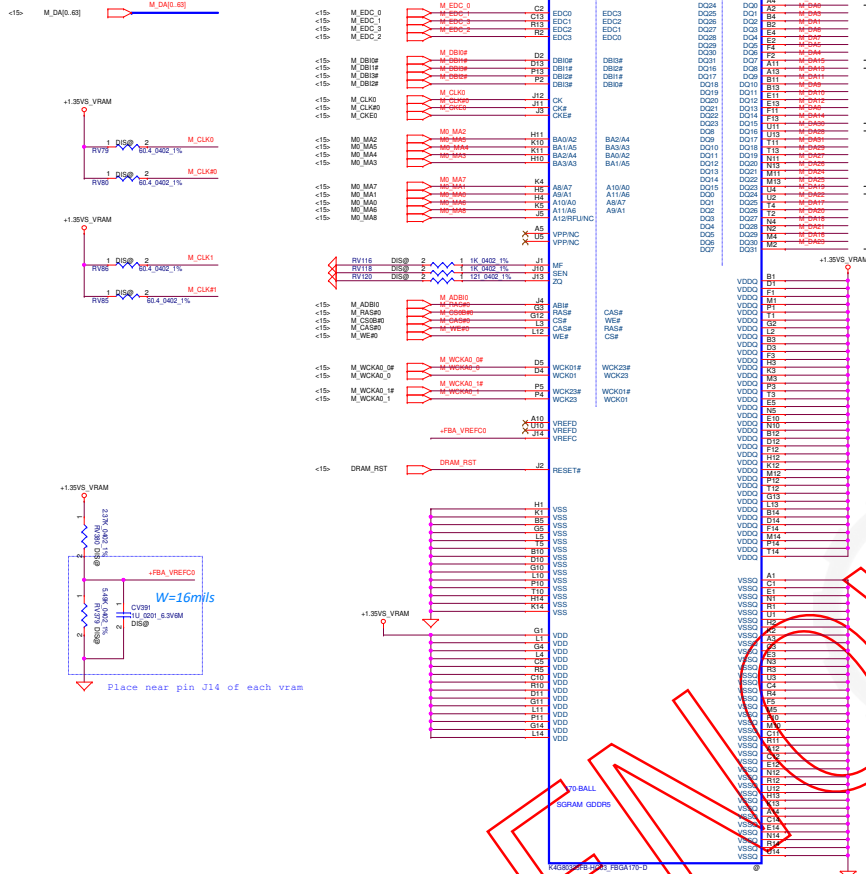
DDR5 Memory Interface:

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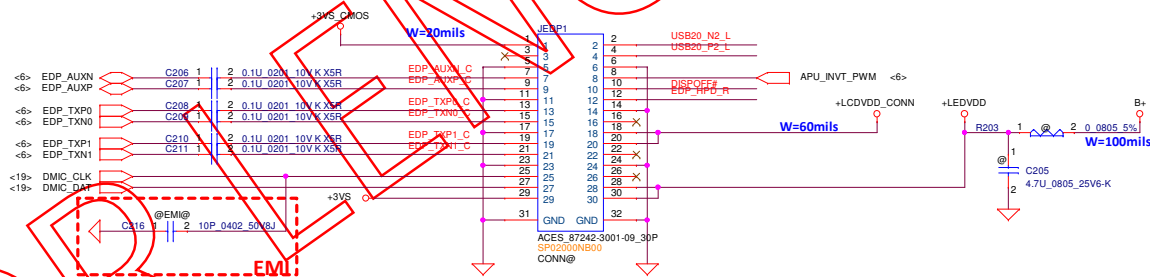
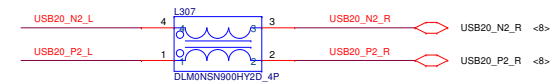
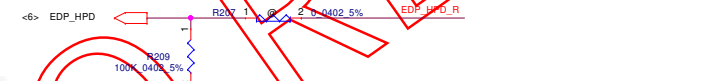
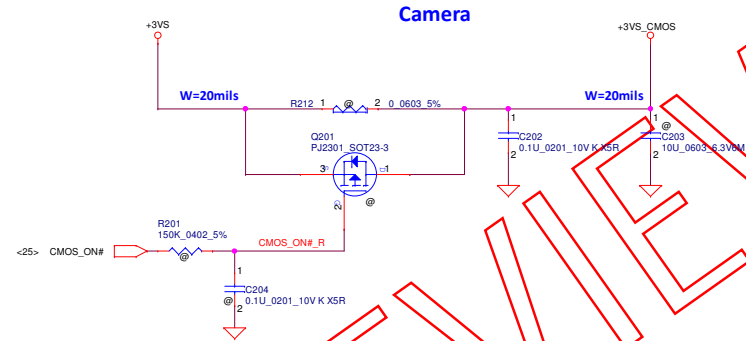
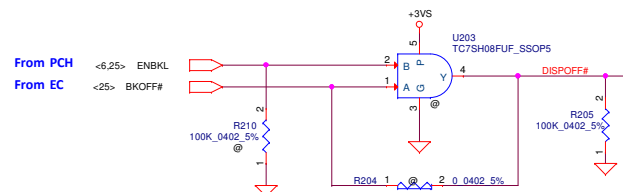
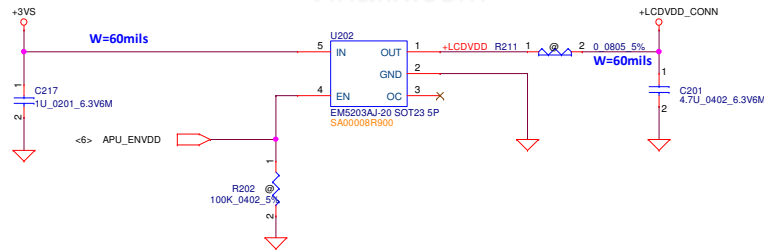
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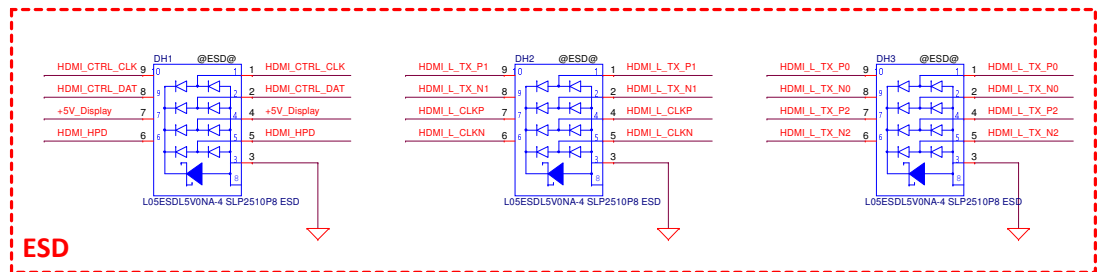
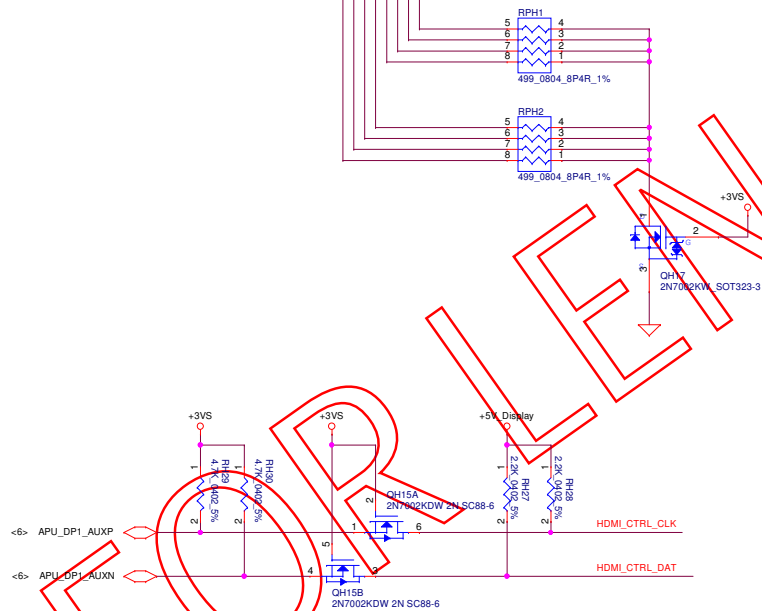
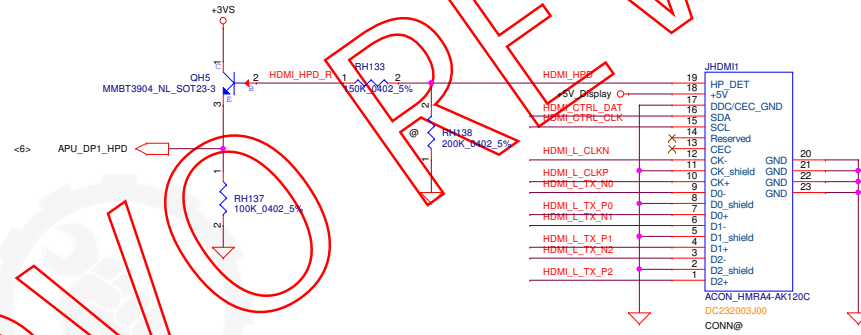
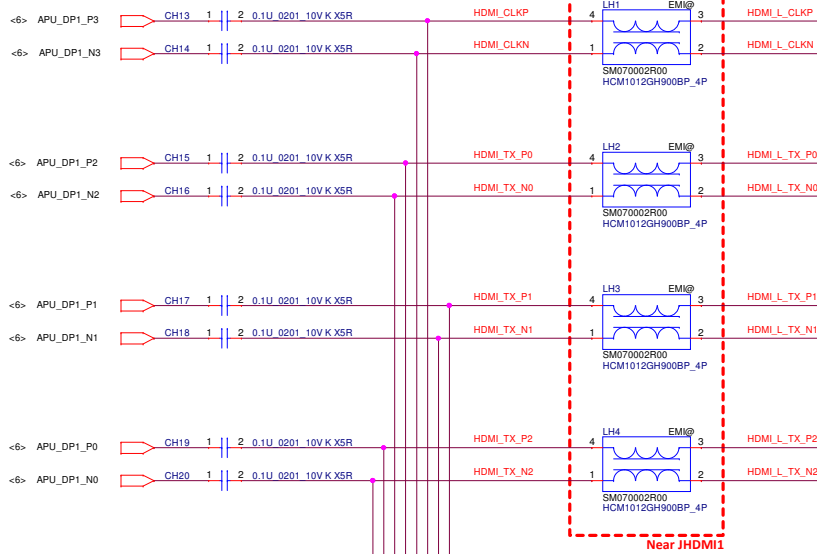
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LCD Power Circuit



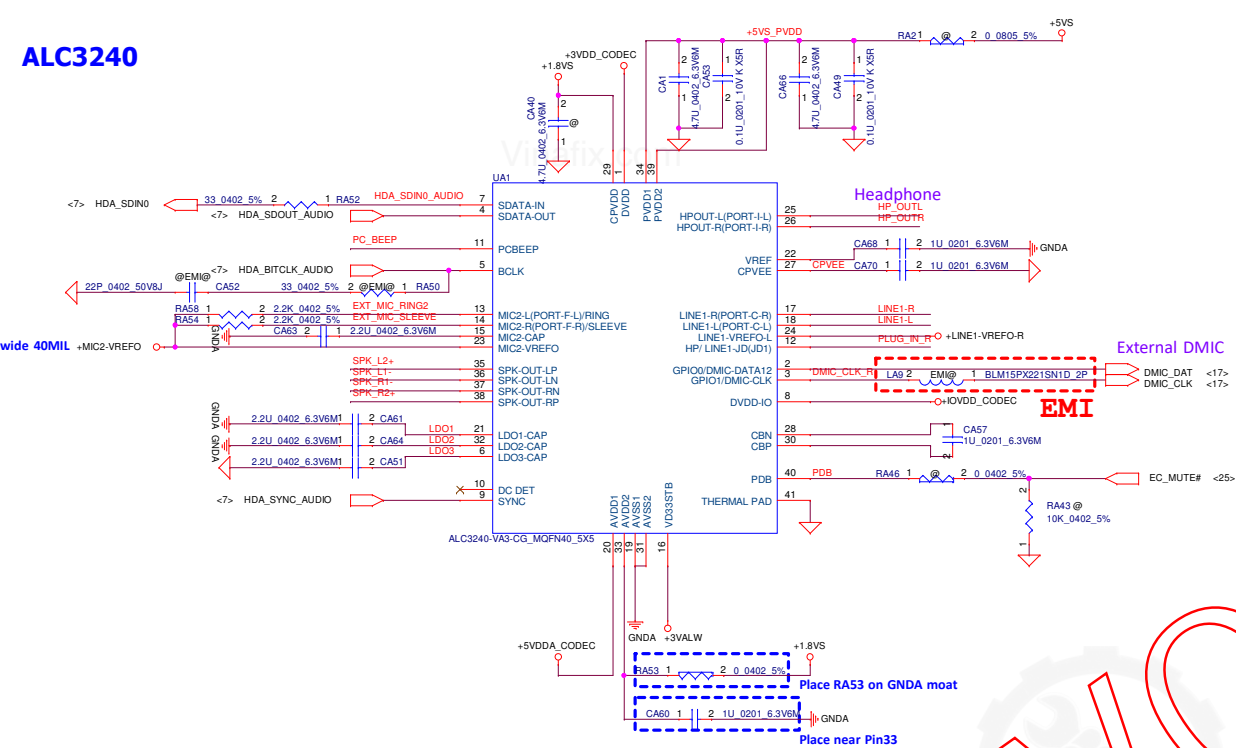
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HDMI

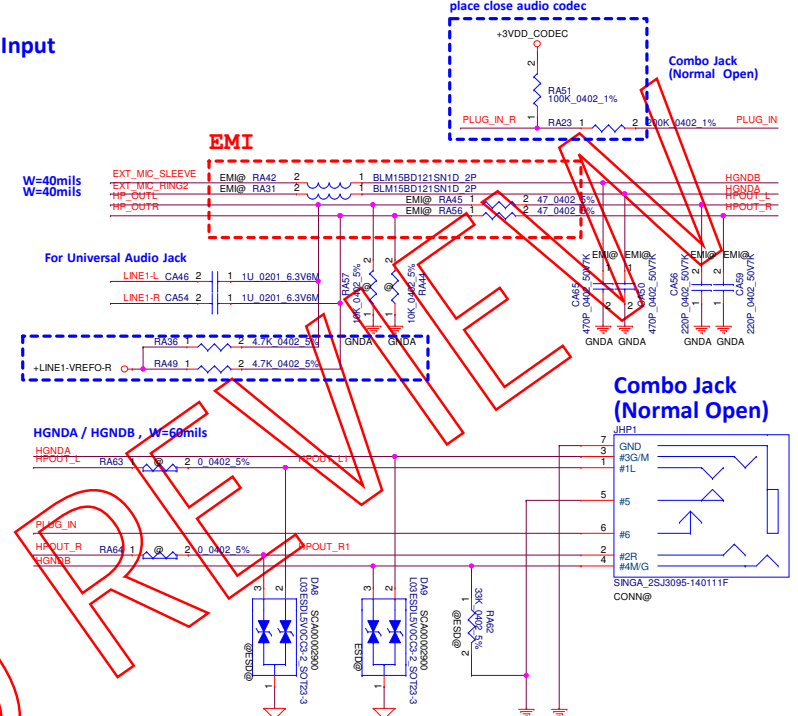


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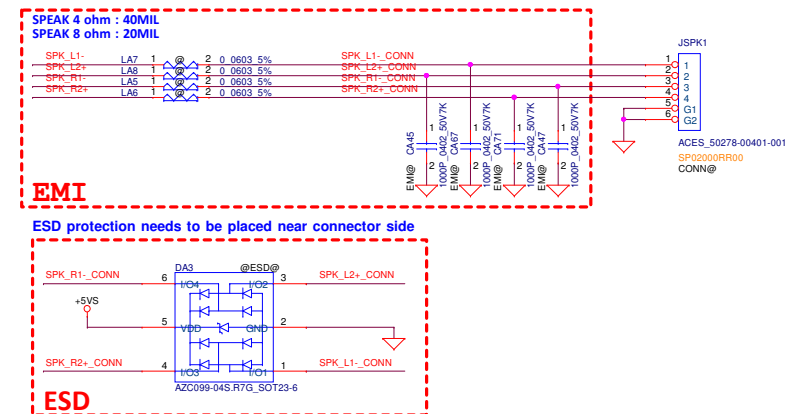
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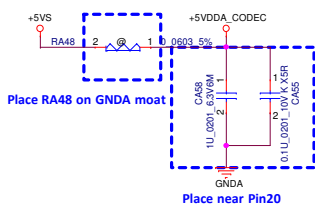
Input



Output



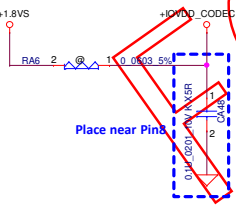
+5VS to +5VDDA_CODEC



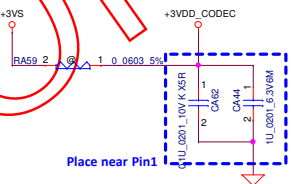
Each Platform HDA Link Voltage Support (Pin 7) :

	3.3V	1.8V	1.5V
AMD Carrizo-L			
AMD Stoney/Radde/F14			

+1.8VS to +IOVDD_CODEC (For AMD FT4)

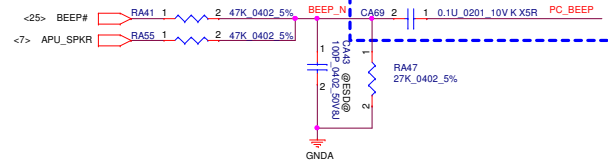


+3VS to +3VDD_CODEC

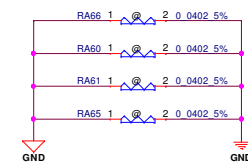


PC BEEP

EC BEEP
APU BEEP

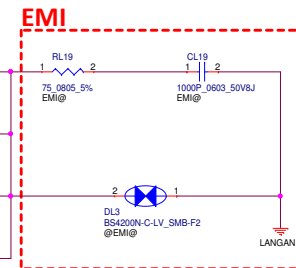
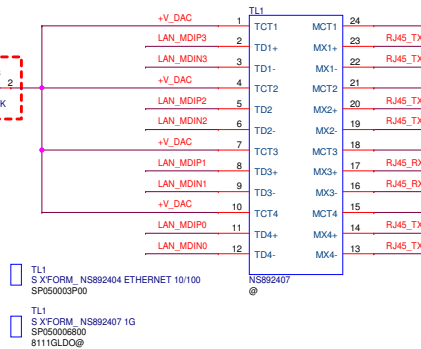
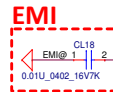
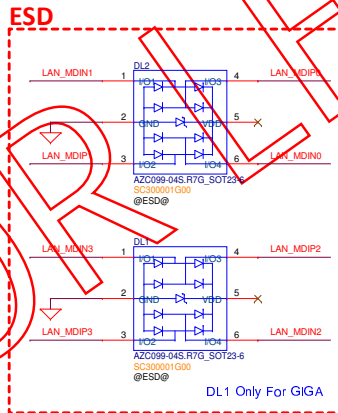
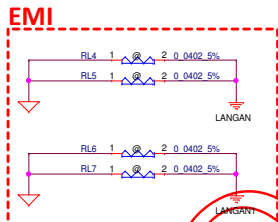
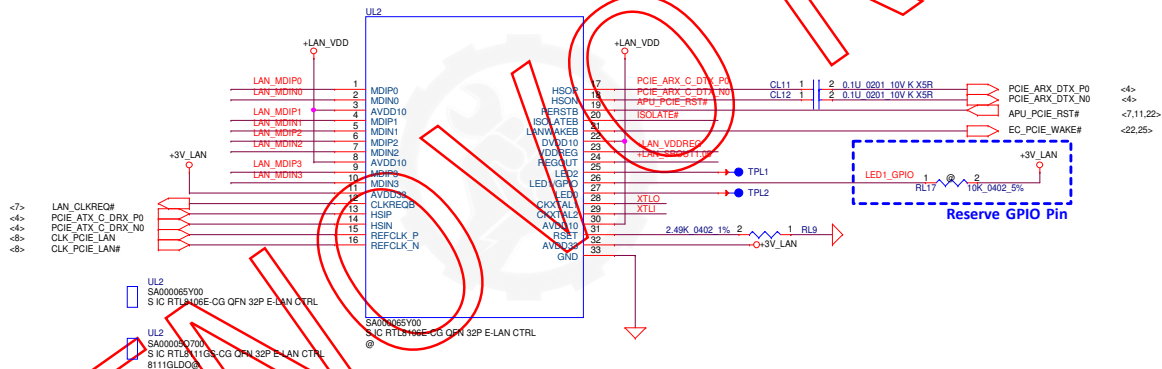
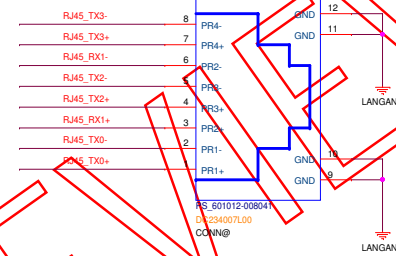
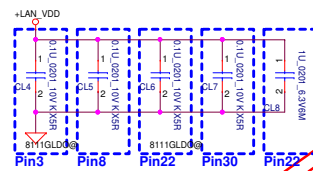
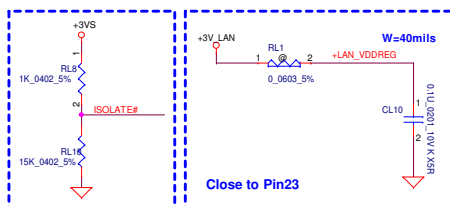
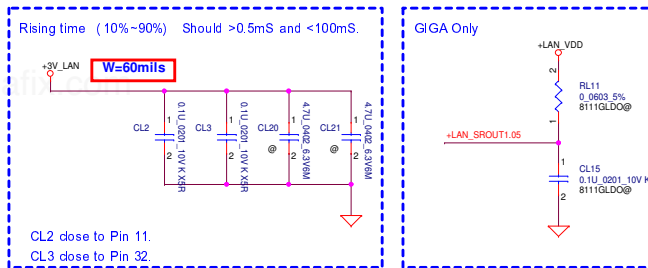
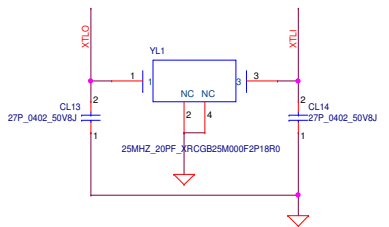
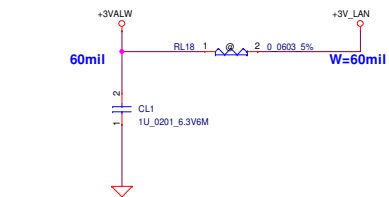


EMI



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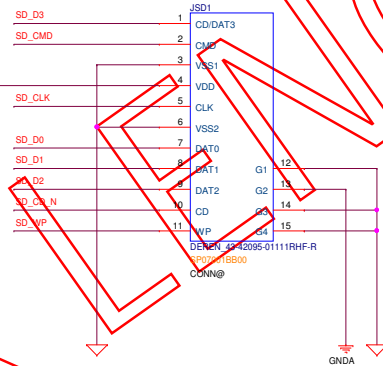
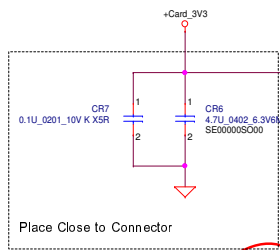
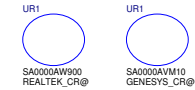
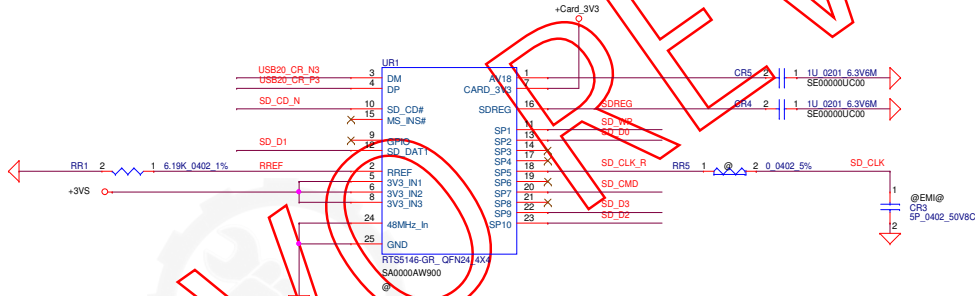
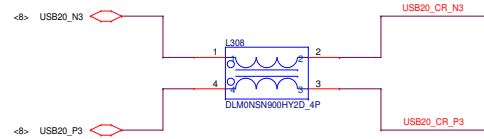
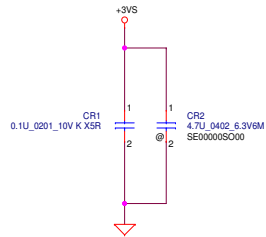
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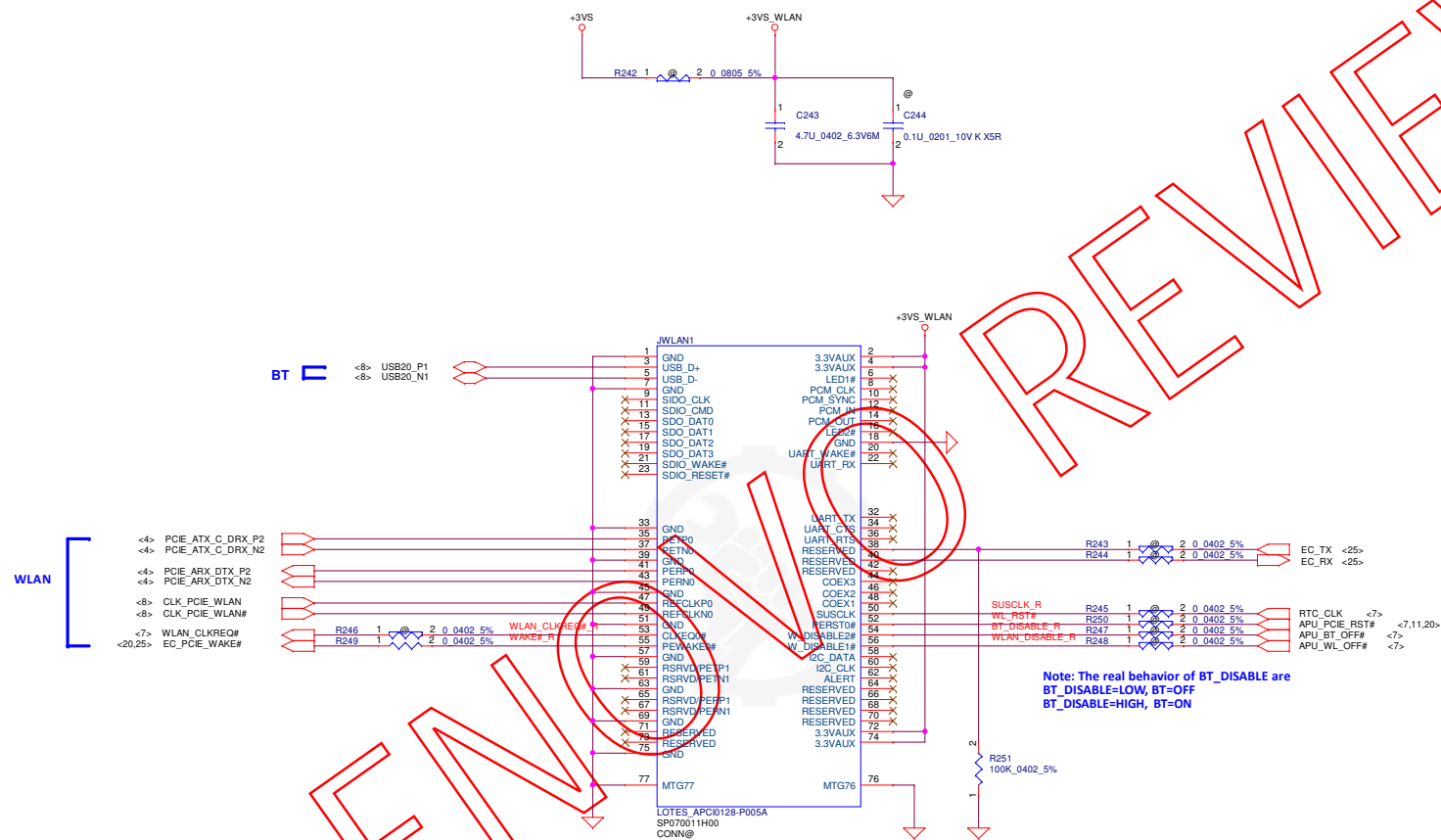
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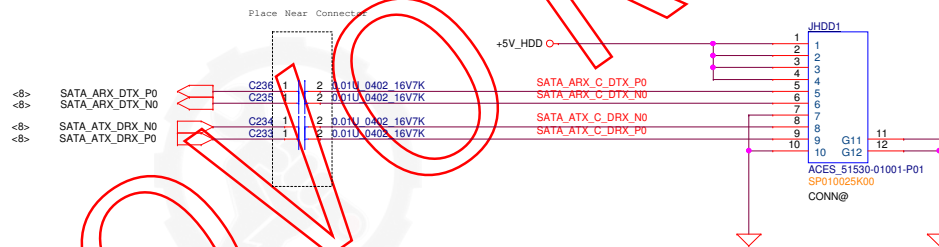
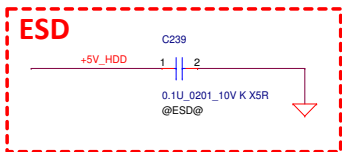
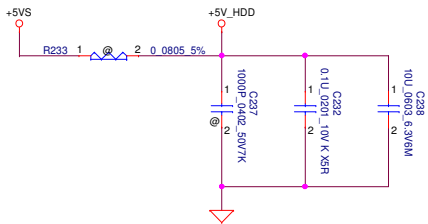
NGFF - WLAN / BT (E- KEY)

Vinafix.com



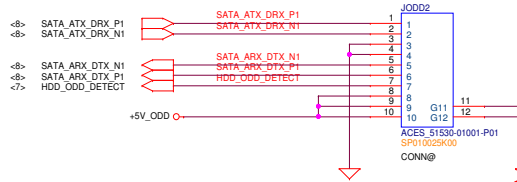
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				Size	Document Number	Rev
					LA-G241P	1.0
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HDD FFC Connector to Sub Board

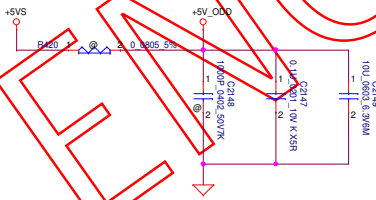


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Size	Document	Number	Rev	LA-G241P		
Custom			1.0			
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ODD FFC Connector to Sub Board (15" Only)

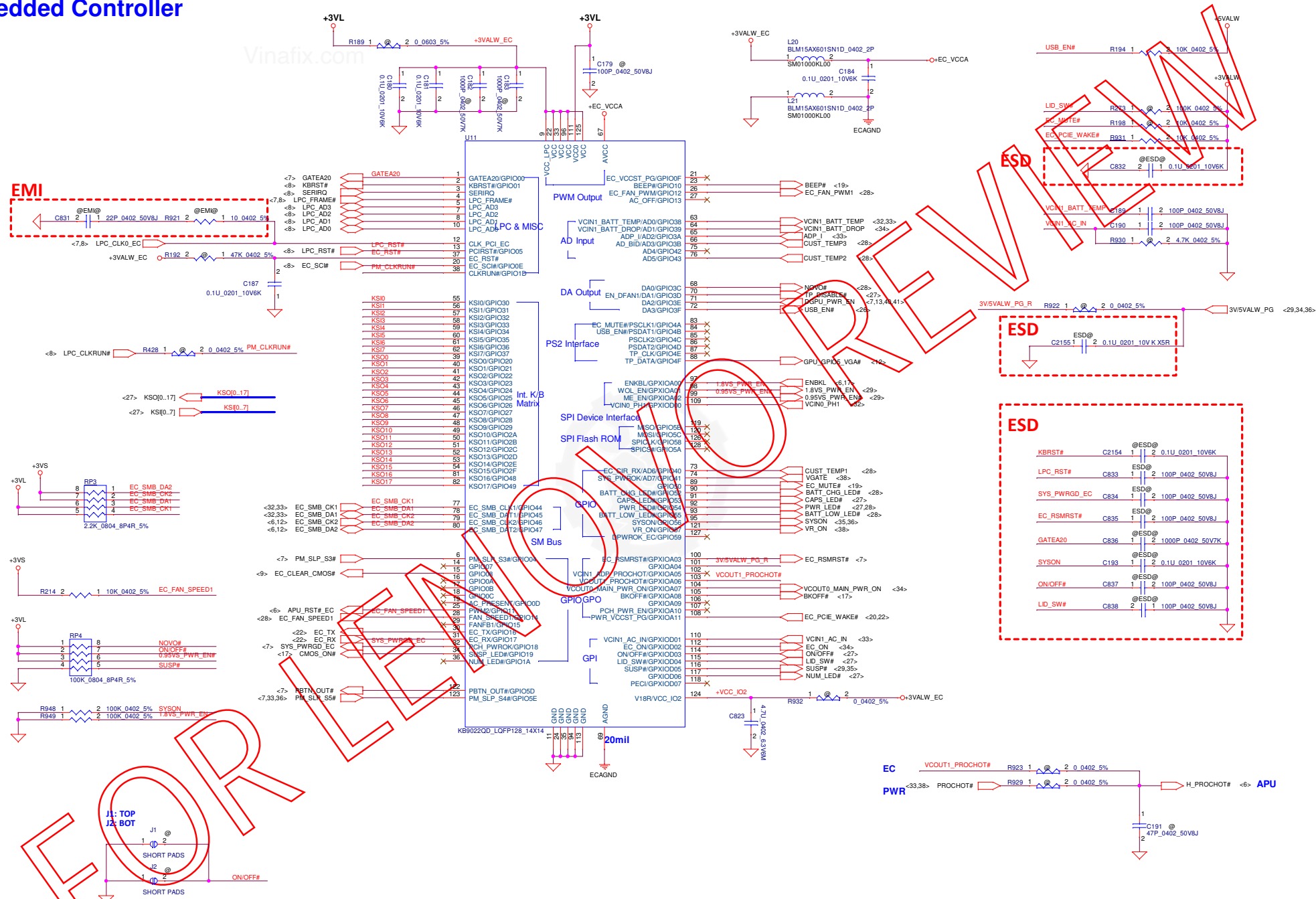


ODD MISC.



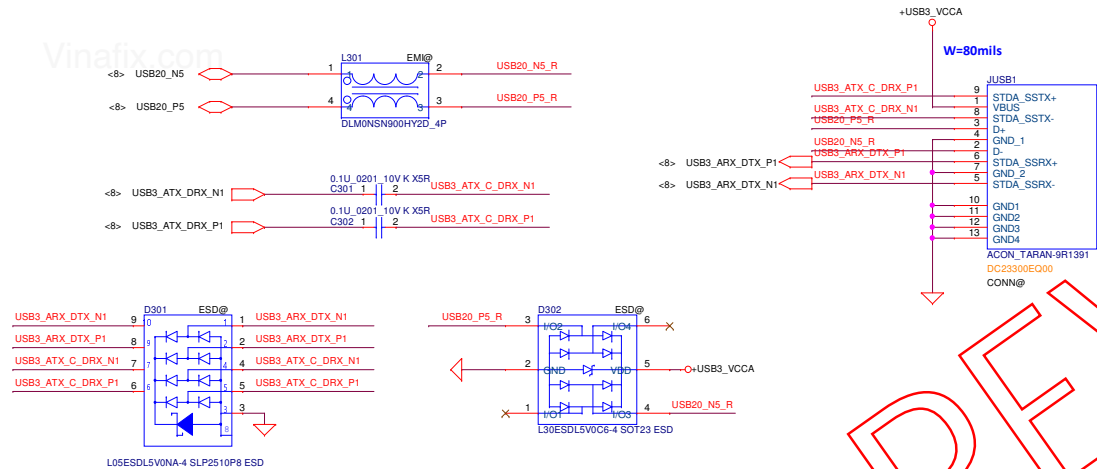
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Embedded Controller

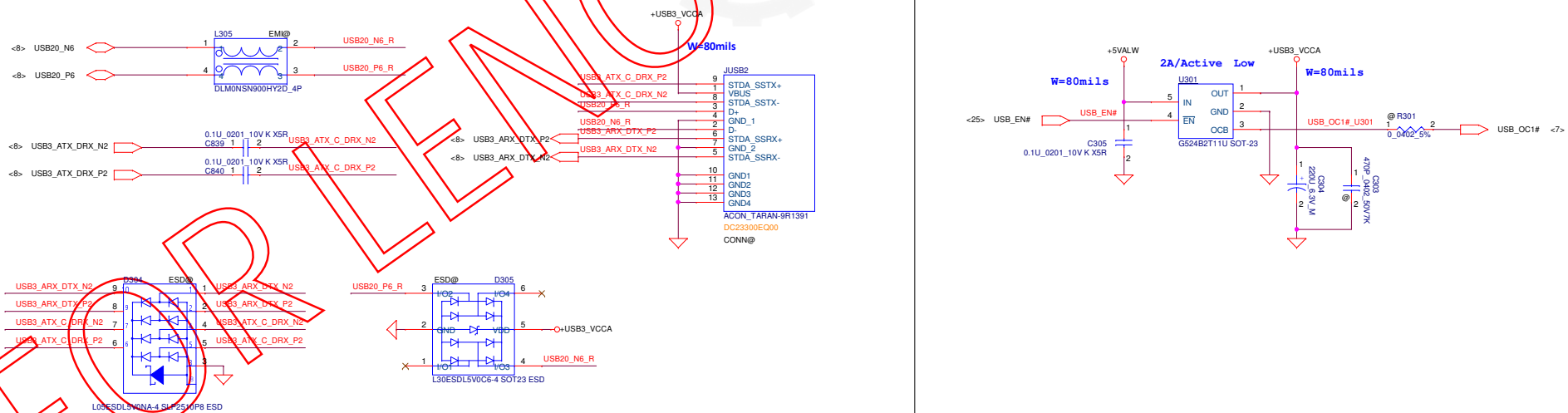


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Issued Date	2018/03/01	Deciphered Date	2019/03/01	Title	
				EC KB9022QD	
				Rev 1.0	
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USB 3.0 (PORT 1)

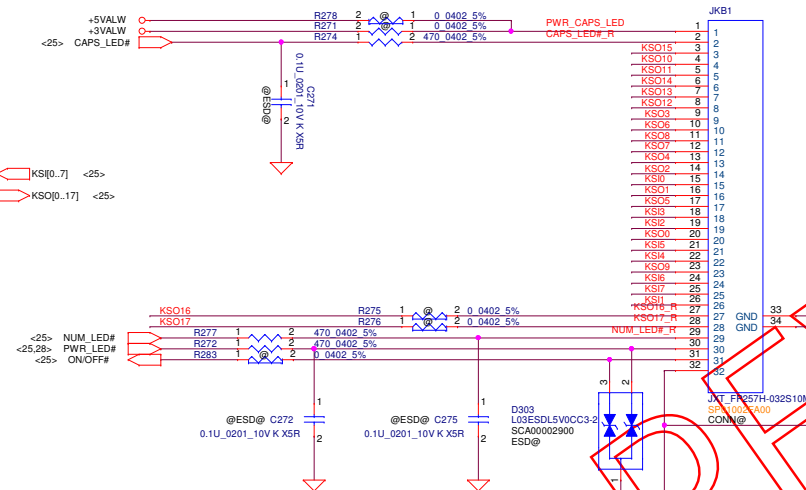


USB 3.0 (PORT 2)

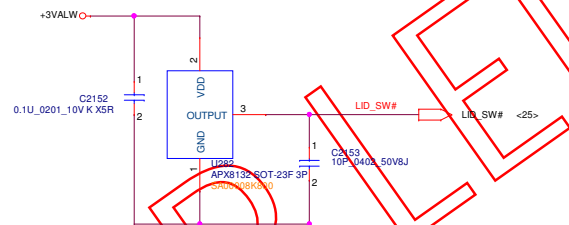


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Issued Date	2018/03/12	Deciphered Date	2019/03/12	USB3.0	
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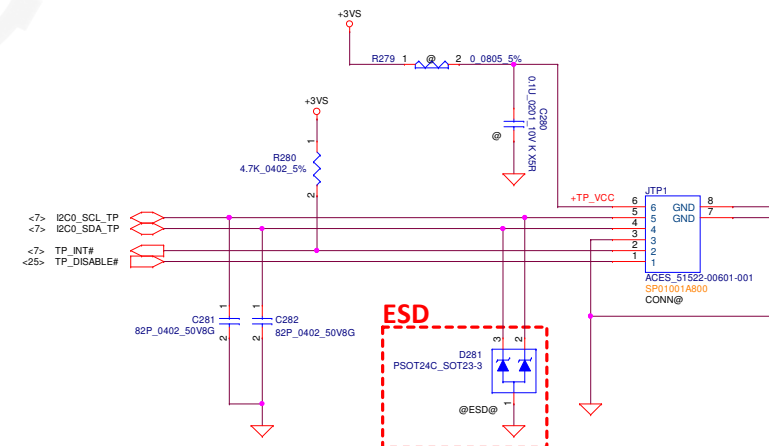
Keyboard



Hall Sensor



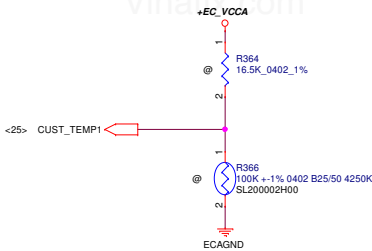
~~TouchPad~~



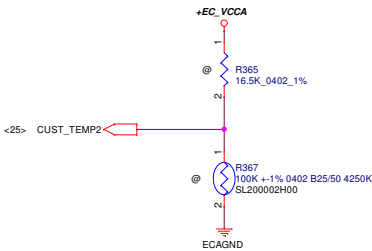
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Thermal Diode

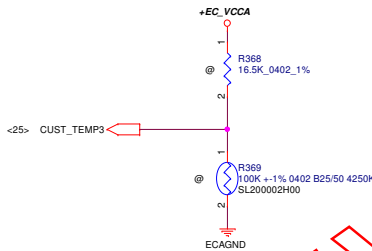
Batt Charge



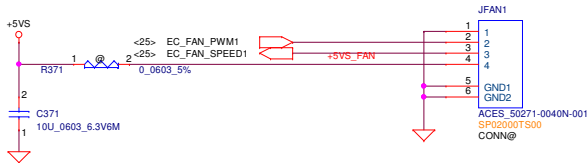
VRAM



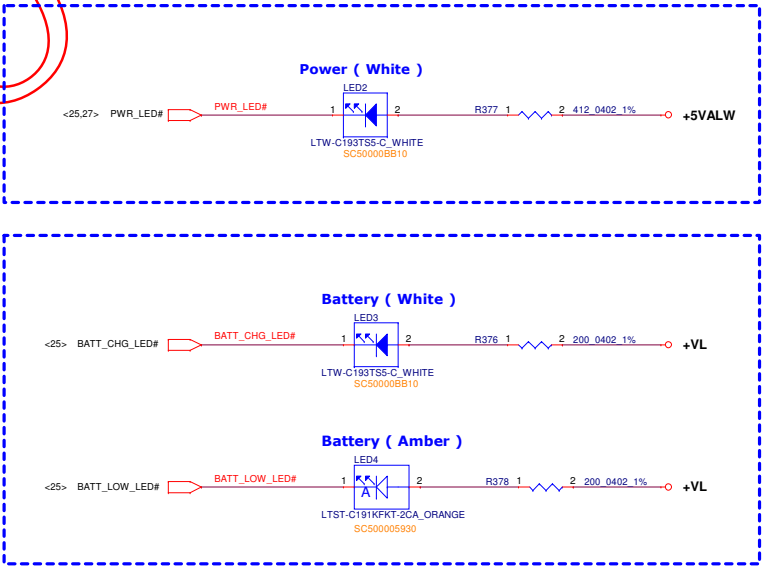
CPU Chock



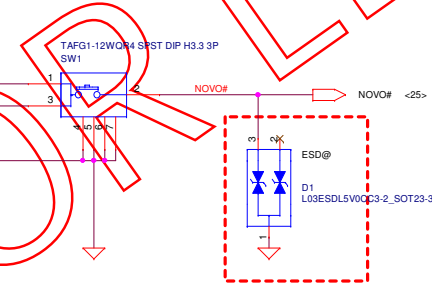
FAN



LED



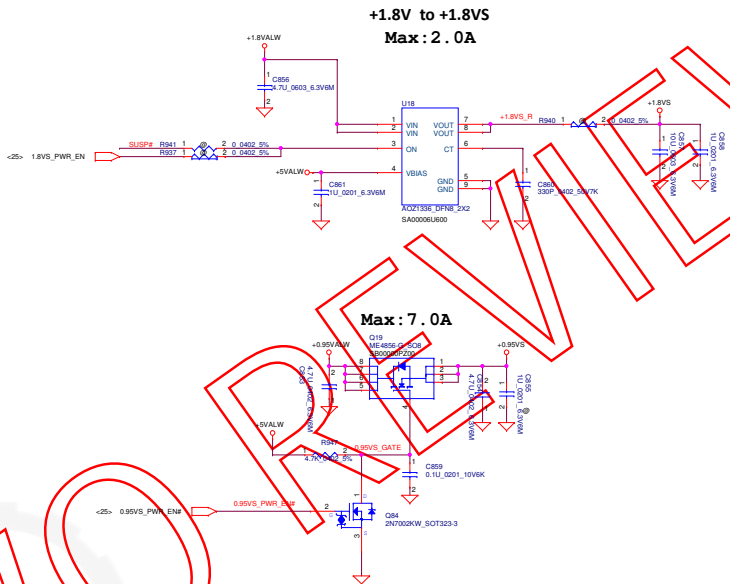
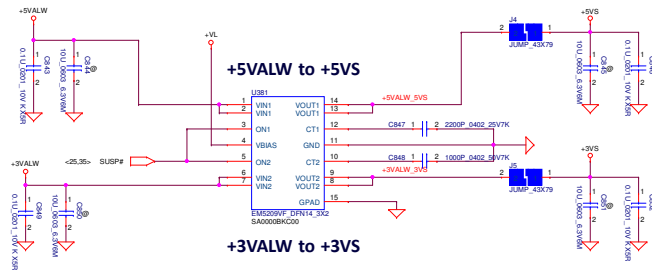
NOVO BUTTON



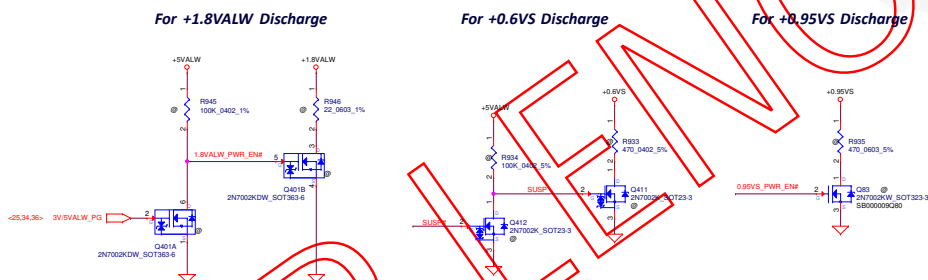
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DC to DC

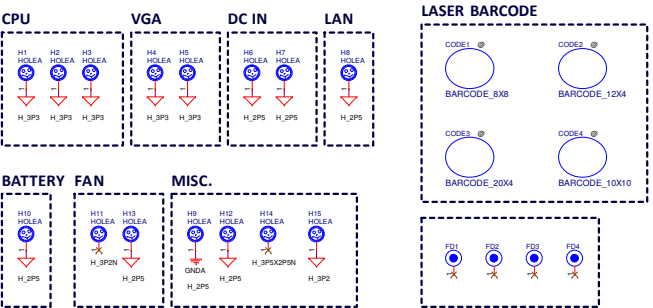
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Discharge Circuit



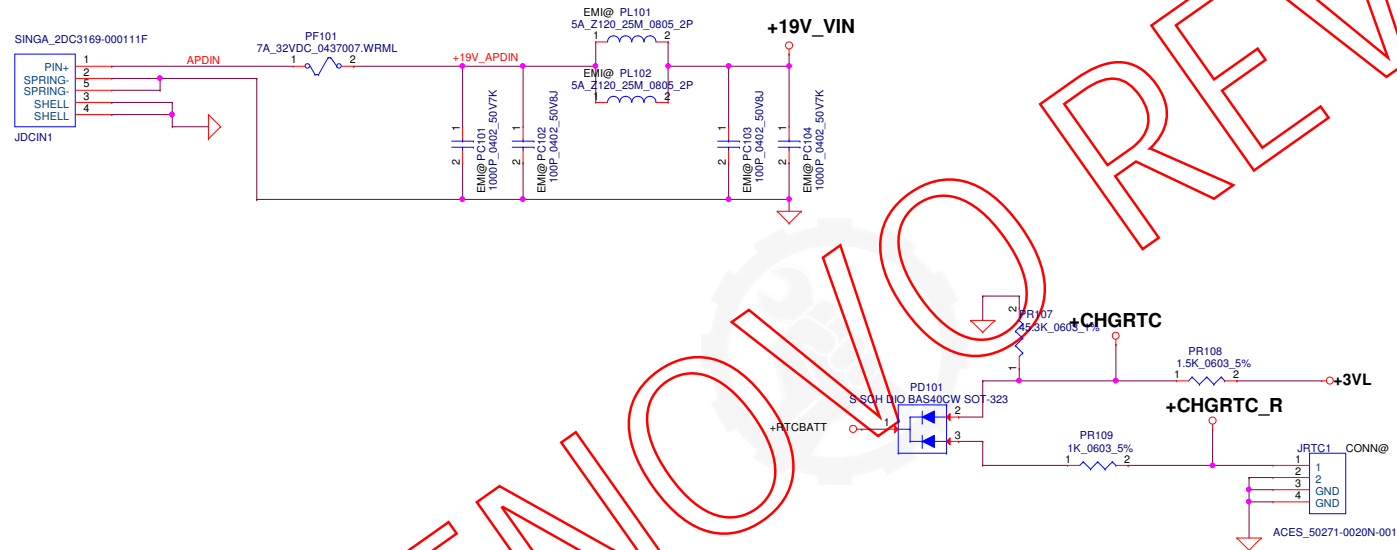
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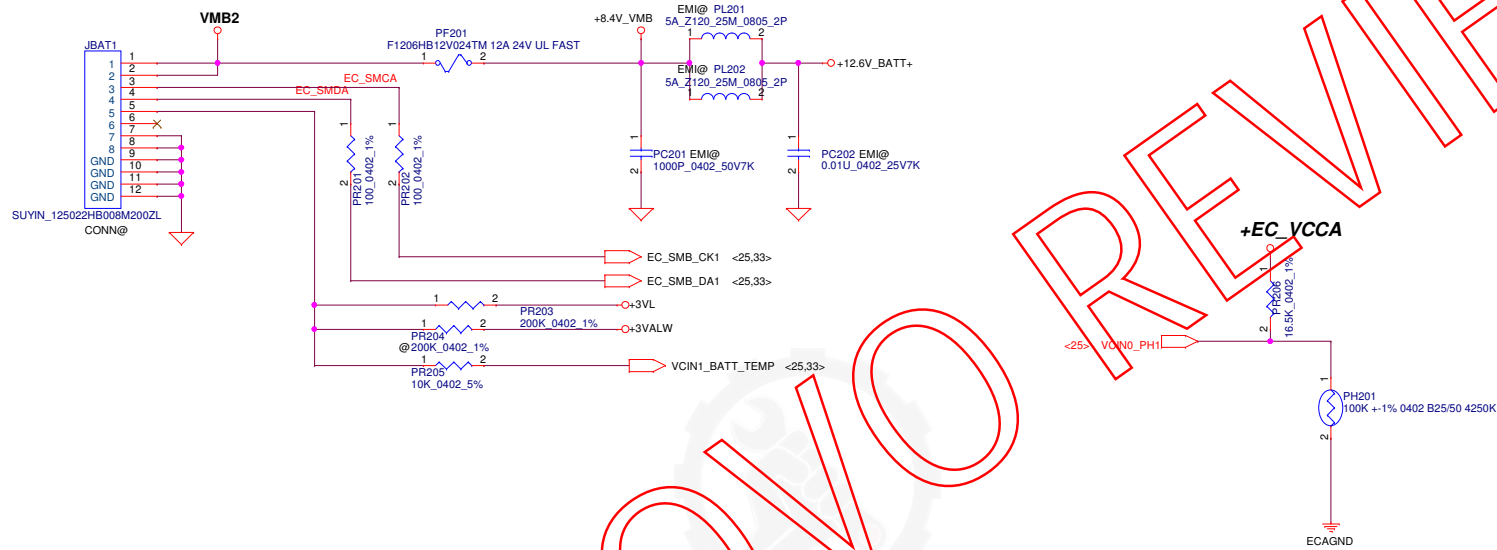
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LA-G241P				28	01

FOR LENOVO REVIEW

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Protection for reverse input

Vgs = 20V
Vds = 60V
Id = 250mA

Rds(on) = 15.8mohm max
Vgs = 20V
Vds = 30V
ID = 10.5A (Ta=70C)

max Power loss 0.22W for 90W; 0.12W for 65W system; 0.05W for 45W
CSR rating: 1W
VCSIP-VCSIN spec < 81mV

Need check the SOA for inrush

PR729 and PR732 are ACDET set ting base on your project to set

0x3CH <BIT9> PSYS current gain
Rs1 = 10mΩ and Rs2 = 5mΩ or Rs1 = 10mΩ and Rs2 = 1mΩ
BIT0 = 1.14uA/W
BIT1 = 0.285uA/W
=====

Rs1 = 20mΩ and Rs2 = 10mΩ or Rs1 = 20mΩ and Rs2 = 2mΩ
BIT0 = 2.28uA/W
BIT1 = 0.57uA/W
=====

Design Notes
For 45W/65W /90W system, 2S/3S/4S battery
Maximum Charging current 3.5A
Maximum Battery discharge power 55W
#Register Setting
1. 0X3DH bit10 set 0 (default 1) to enable turbo boost function
2. Disable turbo when AC only
#Circuit Design
1. ACLIM and CCLIM are divider voltage control.
2. Use 7X7 choke and 3X3 H/L side MOSFET
Charge current 3A
Power loss : 1.79W (H/S=0.227W, L/S=1.2738W, Choke=0.297W)
Power density : 0.61 (23X16)
#Protect function
1. ACOPP : VCC voltage > 24V
2. Smbus timeout : 0X3DH bit5 set 0 (default 0) to enable I2S(default).
3. ACOC : 0X3CH bit4 set release adapter limit function (default:Enable).
4. CHOCO : based on charge current setting
5. BATOVF : 4.6V/Cell
6. BATLOWV : No.
7. TSHUT : 150C

(Rs1 = 10mΩ and Rs2 = 5mΩ or Rs1 = 20mΩ and Rs2 = 10mΩ)
CC_LIM = VccLIM / 64 x Rs2
=====

(Rs1 = 10mΩ and Rs2 = 10mΩ or Rs1 = 20mΩ and Rs2 = 20mΩ)
CC_LIM = VccLIM / 32 x Rs2
=====

AC_LIM = Vac_LIM / 32 x Rs1

Battery current limited by CCLim ~ 3.89A.
Adapter current limited by ACLim ~ 4.33A.
(PR719 and PQ741 are for change ACLim when AC in)

Follow adapter and battery voltage in Vsys current source
Base on CPU Core VR design.
The resistor is pop on CPU VR schematic.

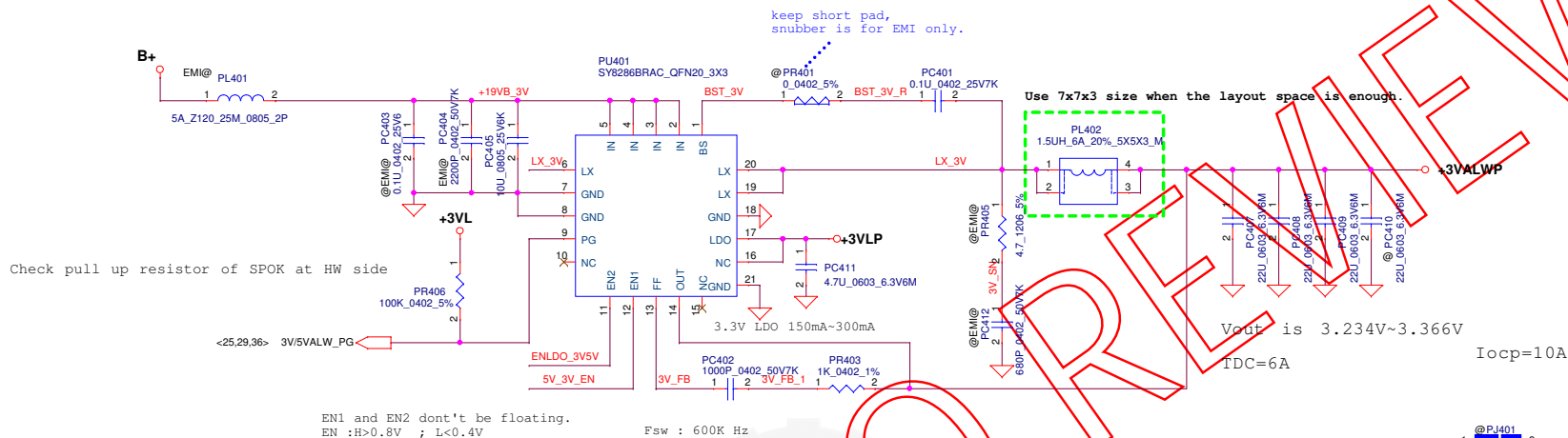
BATGONE (BATT_TEMP)
logic high: above 2.4V
logic low: under 0.8V

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Module model information

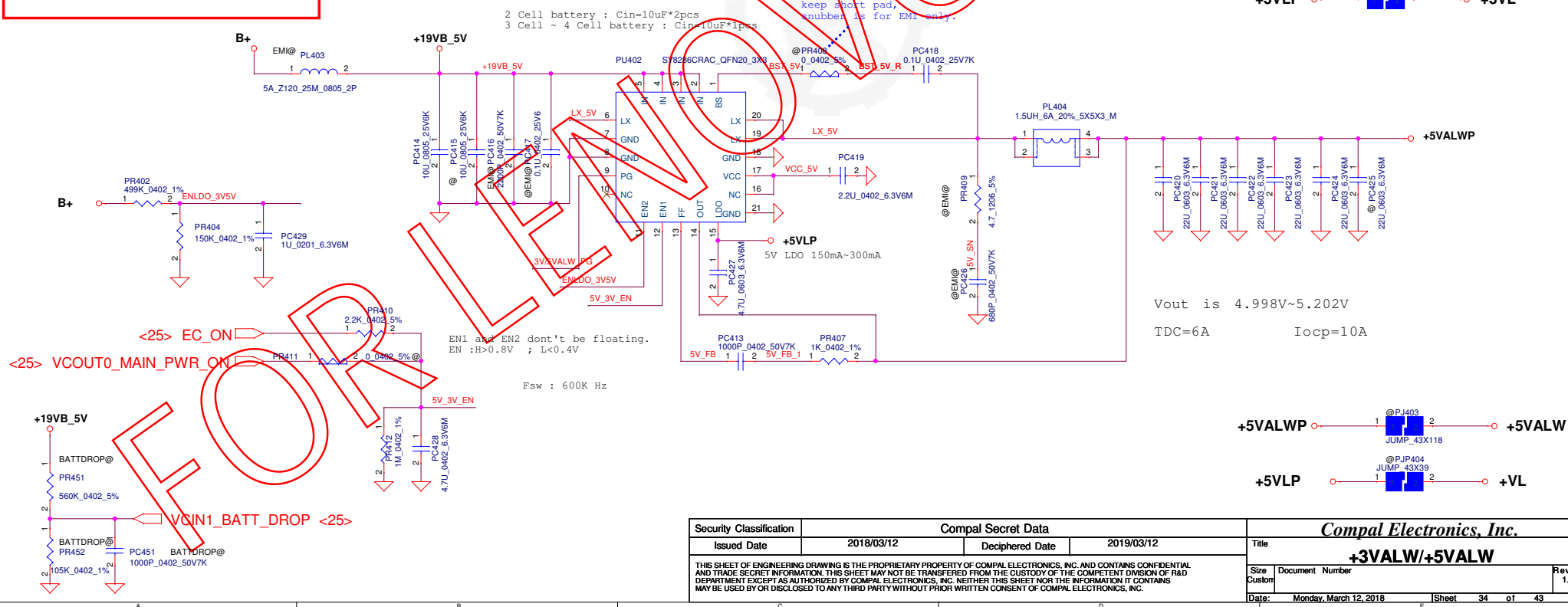
SY8286B_V3_single.mdd
SY8286B_V3_dual.mdd

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Module model information

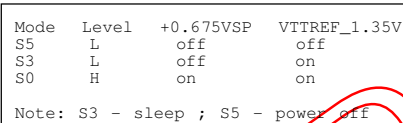
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SY8286C_V3_dual.mdd



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RT8207P_single_V3.mdd	For Single layer
RT8207P_dual_V3.mdd	For Dual layer

0.675Volt	+/-	5%
TDC	0.7A	
Peak Current		1A



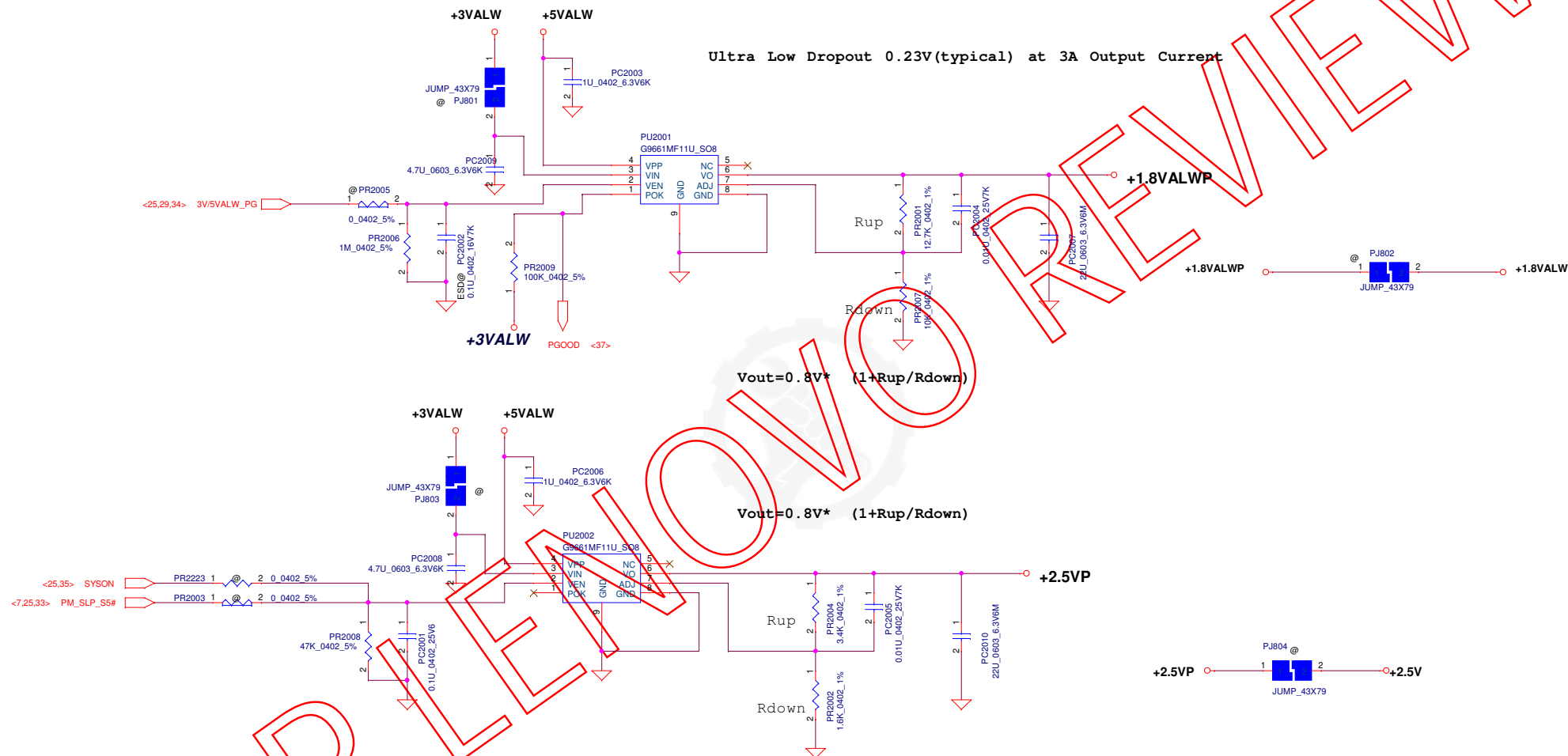
Choke: 7x7x3
Rdc=6.7mohm (Typ) , 7.4mohm (Max)
Switching Frequency: 540kHz
Ipeak=8A
Iocp~9.6A
OVF: 113%~120%
VFB=0.75V, Vout=1.3545V

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Module model information

APL5930_V2.mdd

Ultra Low Dropout 0.23V(typical) at 3A Output Current



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Module model information
RT3661AB_V2A.mdd for IC portion
RT3661AB_V2B.mdd for SW portion

PR816, PR823 are for debug only,
APU_VDD_SEN, APU_VDD_RUN_FB_L need have 10ohm at HW size.

RT3661AB SET1, TSEN and TSEN_NB Pin Setting Function:
AI VDD=100%, AI_VDDNB=100%
OR Threshold: Disable
Frequency: 300kHz
VDD and VDDNB Initial Offset: 0mV (PS0)
VDD and VDDNB PHOCSET Setting Ratio: 150%

$$V_{TSEN_ADC} = 80\mu A \cdot \left[\frac{R_1 \cdot R_{NTC}}{R_1 + R_{NTC}} + \frac{R_{p1} \cdot R_{p2}}{R_{p1} + R_{p2}} \right]$$

$$V_{TSEN_NB_ADC} = 80\mu A \cdot \left[\frac{R_2 \cdot R_{NTC}}{R_2 + R_{NTC}} + \frac{R_{p3} \cdot R_{p4}}{R_{p3} + R_{p4}} \right]$$

APU_CORE_NB
TDC 12A
Peak Current 17 A
OCP current > 25.5A
Load line -4mV/A
FSW=300kHz
DCR 0.98mohm +/-5%
TYP
H/S Rds(on) : 6.7mohm , 8.5mohm
L/S Rds(on) : 3mohm , 3.8mohm

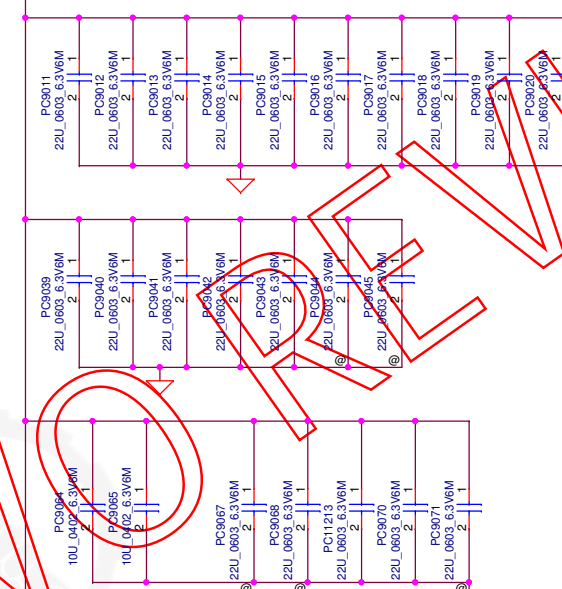
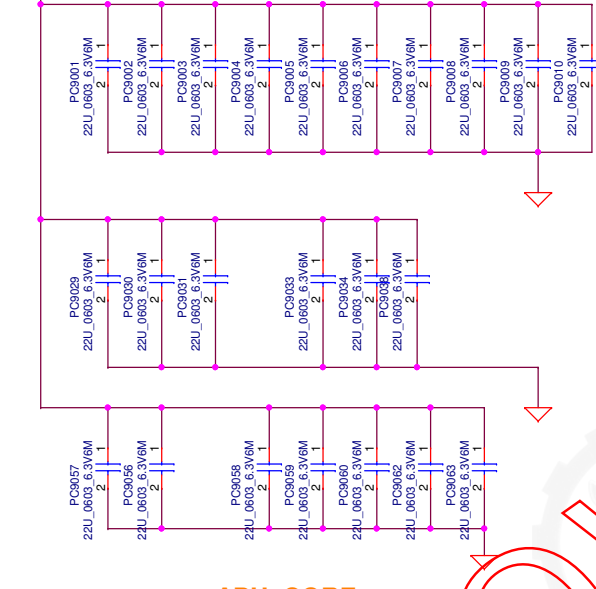
APU_core
TDC 22A
Peak Current 35A
OCP current > 52.5A
Load line -21mV/A
FSW=300kHz
DCR 0.98mohm +/-5%
TYP
H/S Rds(on) : 6.7mohm , 8.5mohm
L/S Rds(on) : 3mohm , 3.8mohm

+APU_CORE

+APU_CORE_NB

+APU_CORE

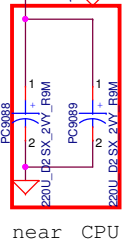
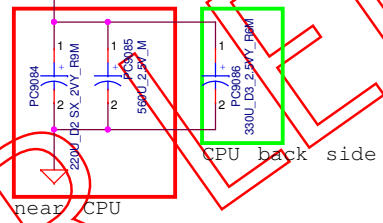
+APU_CORE_NB



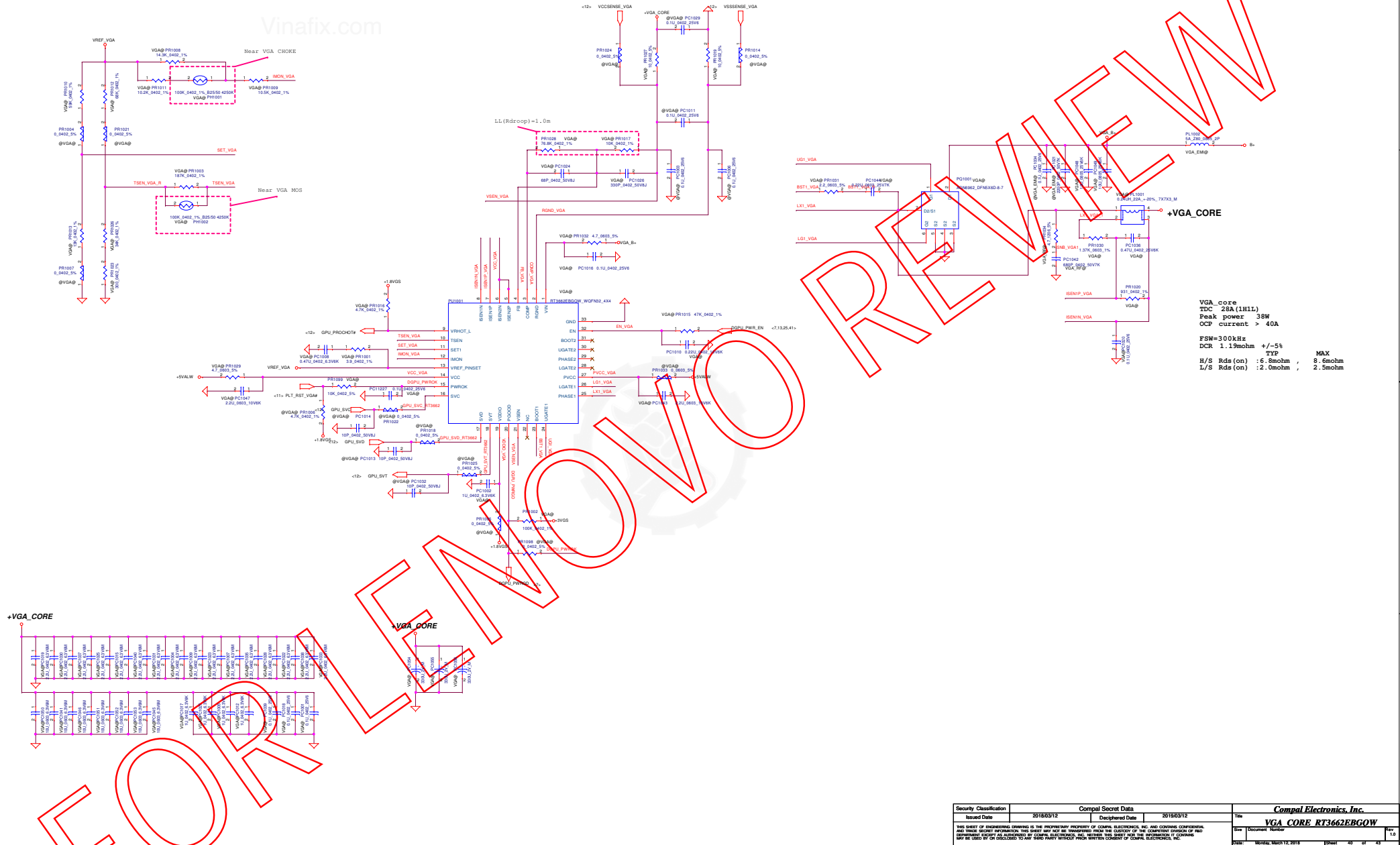
APU_CORE
330uF*3
220uF*1
22uF*23

APU_CORENB
220uF*2
22uF*17+10uF*3

+APU_CORE



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VGA_core
 TDC: 28A(1H1L)
 Peak power: 38W
 OCP current: > 40A
 FSW=300kHz
 DCR: 1.19mohm +/-5%
 H/S: Rds(on): 6.5mohm, 8.5mohm
 L/S: Rds(on): 2.0mohm, 2.5mohm

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